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PLUS:

Tools and Standards Tame System Complexity

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COTS (kots), *n.* **1.** Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. **2.** Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

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Last November Boeing chose the Raytheon Next Generation Radar (RANGR) based on its earlier AN/APG-79 AESA radar for the USAF's F-15E Radar Modernization Program (RMP). Shown here, U.S. Air Force Master Sgt. Jack Braden turns sideways in this self-portrait while riding in an F-16 Fighting Falcon aircraft over training. Braden, from the 8th Fighter Wing's public affairs office, was photographing other aircraft on the training mission.

Courtesy: Master Sgt. Jack Braden, U.S. Air Force.

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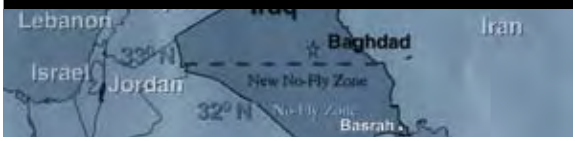

Farnborough's Musical Chairs for the Fighter Programs

It's the summer—time for me to focus on getting up to date on the big military programs and crystal ball what the future holds. For the last few weeks it's been trying to guess what the Farnborough air show would hint for the future of some of the aviation platforms. Running up to the event there's been a lot of news regarding the F-22 Raptor, the F-35 Lightning II, and most recently the F/A-18E/F Super Hornet. Oh, and let me throw in the Su-35 Super Flanker too.

The F-22 and the F-35 are marketed as fifth generation aircraft, with the F-18 being a fourth generation and the Su-35 the fourth and a half—or some other marketing gimmick slogan. Depending on what I read, when I read it, and who wrote it, you get a lot of diverse information. I'm hoping to add to that. It wasn't long ago that I read that the F-22 program was something that the DoD procurement was proud of. Maybe I read that on the Air Force Web site. But I have a tough time buying into that concept—unless you go by some mystical equation that I've never heard mentioned like percentage cost overrun per year divided by performance mitigations and so on. Depending on where you look—and how you interpret the shell game that's played with the final cost—the F-22 "fly away" price will be starting anywhere from $140 million each.

The F-22 is the latest wiz bang that we've designed for air-to-air combat. It can do supporting roles, and most recently the Air Force wanted to ship some to Iraq to perform "surveillance" missions. The DoD and Congress nixed this idea probably for more reasons than politics—could even have been common sense. Instead, the F-22 made its European curtain call at Farnborough, for a whole 12 minutes…Now you see it now you don't. I guess the F-22 boys wanted to outdo the Russians who held a private, by invitation, in country showing of its Su-35 that was reported to have lasted just about 6 minutes. The Russians feel that the Su-35 is a strong competitor to the F-18 and the Eurofighter Typhoon. They don't have any ITAS issues to contend with and are going to price it about 30% less than the F-18.

Where does the F-35 fit into all of this? The F-35 is really not developed for air-to-air superiority. That leads me to wonder why it wasn't designated F/A-35—please don't e-mail me on this comment, I know it's a cheap shot. The F-35 is really designed for multirole missions from bombing to close air support. That's not as glamorous a role as envisioned for the F-22, and I'm sure there are people in the Air Force who aren't happy about the reduction in glamour the F-35 will deliver. All that said, the intent of the F-35 is to get a fifth generation aircraft that is affordable through volume production. The most recent target price for the non-naval, non-STOVL version F-35A is somewhere in the range of $50 million when at "full production."

Now all the players with a stake in these aircraft are in a free-for-all. We have countries' military organizations, these countries' politicians and the manufacturers all trying to leverage their point of view. I think Congress is pushing the F-35 but I'm never sure. They think that they gave the Air Force enough F-22 toys to play with. The DoD is definitely pushing for the F-35. The Air Force wants more F-22s, but they know they're never going to get them. All this outside pressure has the F-35 lead contractors at Farnborough telling all the countries participating in the F-35 development that it's now or never for all the potential buyers to commit to quantities. They'll let buyers lock in a price, but it's a firm commitment. If you fail to take your commitment, you must pay all the other guys that have committed their difference in the increased price because of your failure. That's going to go over like a lead balloon for all the countries playing with its development. What if in the next ten years there are different politicians in power? What if, what if….

The most interesting thing coming out of Farnborough is something that has been elusive for decades. It's been tried several times and has fallen flat at each and every attempt: the Multirole Missile. Three companies—Lockheed Martin, Northrop Grumman and Alliant Techsystems—announced that they have agreed to an equal partnership in the development and production of the missile. The companies feel that technology has advanced enough where this can actually be developed and produced, and that they have figured out how to do it. When this becomes available it will be exactly what all stealthy aircraft with internal payloads need: one piece of ordinance rather than two. Right now one piece is required for defense and the other for mission accomplishment. In contrast, the pilot would determine this Multirole Missile's mission when the need developed using only one device to either shoot down an aircraft or hit a target on the ground. Will this help the F-22? The question in this game of musical chairs may not be what music is playing but who actually is controlling the switch. ▮▮

Pete Yeatman, Publisher
COTS Journal

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The Inside Track

VMETRO Deploys Storage System on Navy Helicopter

VMETRO has shipped data recording solutions to the Radar Systems Division of Telephonics, a wholly owned subsidiary of the Griffon Corporation, for the US Navy MH-60R (Figure 1) Multi-Mode Automatic Radar Periscope Detection and Discriminator (AR-PDD) program. The data recording solutions are based on VMETRO's Vortex Open Data Recording platform and SANbric rugged rotating media storage device. VMETRO developed a Shock Isolation Unit (SIU) for deployment of two SANbric storage devices as well as application-specific software. The SIU that was developed for this application was designed and tested to meet the shock and vibration profile supplied by the customer. The SIU holds two SANbric units for an aggregate maximum recording rate of 720 Mbyte/s and 3.6 Terabytes of recording capacity.

The SANbric is a sealed metal enclosure housing up to six high-performance hard drives. The unit makes use of dual-port, enterprise-class, Fibre Channel drives, allowing high-speed data recording in high-altitude rugged environments. The Shock Isolation Unit (SIU) is designed to isolate the SANbric from harsh operating environments. Each SANbric is shipped in an individual case with custom foam, wheels and extendable handle for easy transport and shipping. The SANbric uses two 50-pin D-subminiature (DD-50) connectors on the rear of the unit for blind mate connection when inserted into its chassis. One connector provides power and console port communication, while the other contains the Fibre Channel ports.

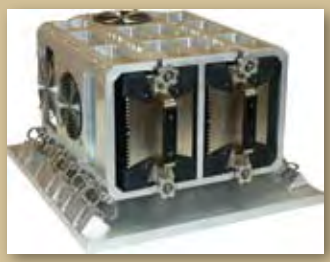

Figure 1

Previously known as SH-60R, this helicopter was renamed MH-60R (left) to reflect its multi-mission role. VMETRO developed a Shock Isolation Unit (SIU) (right) for Telephonics that comprises two SANbric units for an aggregate maximum recording rate of 720 Mbyte/s and 3.6 Terabytes of recording capacity.

VMETRO
Houston, TX.
(281) 584-0728.
[www.vmetro.com].

Saft Wins $170 Million Li-$SO_2$ Battery Contract

Battery manufacturer Saft has been awarded a major multi-year contract by the U.S. Defense Logistics Agency (DLA) to supply the U.S. Army, Navy, Air Force and Marine Corps with BA5590 lithium sulfur dioxide (Li-SO_2) batteries. The terms of the contract include Li-SO_2 batteries for several portable military applications such as communications and electronics systems.

This contract was awarded to Saft for 100 percent of the U.S. military needs for this type of battery. The contract with DLA is an indefinite quantity contract with a two-year base period for an amount of up to $64 million and three one-year option periods for a total contract value of up to $170 million. Orders under the contract are demand-based, with the first one expected toward the end of 2008.

Saft America
Cockeysville, MD.
(410) 771-3200.
[www.saftbatteries.com].

Curtiss-Wright Awarded $4.25 Million Ethernet Switch Contract for FCS

Curtiss-Wright Controls was chosen for the development and demonstration phase of the U.S. Army's Future Combat Systems' (FCS) Integrated Computer System (ICS) program. Under terms of the contract with General Dynamics C4 Systems and Rockwell Collins, Curtiss-Wright will supply its Gigabit Ethernet Switch Module (GESM) to the program. General Dynamics and Rockwell Collins provide the computer processing, networking, information assurance and data storage resources necessary to support the network-centric operations of FCS (Figure 1).

Figure 2

The Gigabit Ethernet Switch Module will be used in several FCS vehicles. Shown here is the XM1203 Non Line of Sight-Cannon (NLOS-C) after product. It is an indirect fire support component of the Manned Ground Vehicle (MGV) family.

The GESM contract will be fulfilled by the Curtiss-Wright Motion Control segment facility in Ottawa, Canada and shipped to Rockwell Collins. Curtiss-Wright will supply the General Dynamics/Rockwell team with a rugged VPX-based line replaceable module called the VPX3- 683. VPX3-683 technology supports "in-

the-field" servicing, enabling the replacement of individual cards rather than entire card-filled subsystems, thus reducing cost, complexity and logistics. The award also includes a services contract to be provided by Curtiss-Wright with a production phase option planned to start in 2010.

Curtiss-Wright Controls
Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

SprayCool Contracted for Predator SIGINT Application

Northrop Grumman Corporation's ISR Systems Division has awarded SprayCool a contract to provide its liquid-cooled enclosures for

Figure 3

SprayCool enclosures will house SIGINT electronics for the Air Force's SIGINT-equipped MQ-1B Predator UAV. The Predator is a medium-altitude, long-endurance, remotely piloted aircraft.

the U.S. Air Force Airborne Signals Intelligence Payload 1C (ASIP-1C) program. The SprayCool enclosures will house SIGINT electronics for the Air Force's SIGINT-equipped MQ-1B Predator UAV (Figure 3) in support of Predator's tactical warfighting role, sometimes described as a hunter/killer/scout mission.

Under this contract, the SprayCool Multi-Platform Enclosure (MPE) was selected by Northrop Grumman as a critical component in the ASIP-1C sensor payload for SIGINT-equipped Predator aircraft. Additionally, the SprayCool selection allowed Northrop Grumman and the Air Force to leverage their previous investment by enabling them to use the same electronics that are on the baseline ASIP program on other platforms.

Meanwhile, in other SprayCool news, GE Fanuc Intelligent Platforms has signed an agreement with SprayCool that enables GE Fanuc to act as a supplier of fully integrated subsystems that include GE Fanuc's off-the-shelf embedded computing solutions within a SprayCool chassis.

GE Fanuc Embedded Systems
Charlottesville, VA.
(800) 368-2738.
[www.gefanucembedded.com].

SprayCool
Liberty Lake, WA.
(509) 232-2600.
[www.spraycool.com].

Navy Taps L-3 for Rugged Shipboard Navigation Systems

L-3 Advanced Products & Design has been awarded a five-year, $16 million indefinite-delivery/indefinite-quantity (ID/IQ) contract for the production and delivery of Navigation Sensor System Interface (NAVSSI) system racks, kits, parts and production engineering services support. The contract was awarded by the Space and Naval Warfare Systems Command in San Diego, CA.

The NAVSSI system collects, processes, integrates and formats the distribution of Precise Navigation and Timing (PNT) data to weapon systems, combat support systems, C4ISR systems and other information systems aboard various ship classes. This contract combines purchases for the U.S. Navy and the governments of Australia and Spain under the Foreign Military Sales Program.

L-3 Communications
San Diego, CA.
(800) 621-8474.
[www.l-3com.com/apd].

Navy Awards General Dynamics $23 Million for DMR Shipboard Radios

General Dynamics C4 Systems has been awarded a $23 million contract for AN/USC-61(C) Digital Modular Radios (DMRs), the Navy's standard communications system for newly constructed ships and submarines. Deliveries are scheduled to begin in mid-2009 and continue though 2010. The software-defined DMRs (Figure 4) communicate with Ultra-High-Frequency SATCOM, Single-Channel Ground and Airborne Radio Systems (SINCGARS), Line of Sight and High-Frequency radios on Navy surface and subsurface platforms.

General Dynamics has delivered more than 370 DMRs for use throughout the fleet and at Navy shore sites, enabling secure short-range and global communications using U.S. military standard waveforms. General Dynamics C4 Systems delivered the first Digital Modular Radio to the Navy in 1998; it was one of the first software-defined radios to be delivered under contract to

Figure 4

The software-defined Digital Modular Radios (DMRs) communicate with Ultra-High-Frequency SATCOM, Single-Channel Ground and Airborne Radio Systems (SINCGARS), Line of Sight and High-Frequency radios on Navy surface and subsurface platforms.

the U.S. military. In October 2004, the radio became the first software-defined radio certified by the National Security Agency for communications up to the Top Secret level. The DMR contracting office is the Space and Naval Warfare Systems Command, working on behalf of the Program Executive Office for Command Control Communications Computers and Intelligence, San Diego, CA.

General Dynamics C4 Systems
Scottsdale, AZ.
(480) 441-3033.
[www.gdc4s.com].

COTS Websites

www.acq.osd.mil/dpap

DPAP Web Site Is Grand Central for Defense Procurement Info

Defense procurement with all its associated policies and regulations is a complex beast to keep on top of. Fortunately, the office of Defense Procurement, Acquisition Policy, and Strategic Sourcing (DPAP) provides a website that helps organize and facilitate the system. The DPAP is responsible for all acquisition and procurement policy matters in the Department of Defense (DoD). The DPAP office serves as the principal advisor to the Under Secretary of Defense for Acquisition, Technology and Logistics (AT&L), Deputy Under Secretary of Defense for Acquisition and Technology (A&T), and the Defense Acquisition Board on acquisition/procurement strategies for all major weapon systems programs, major automated information systems programs and services acquisitions.

The DPAP website provides a wealth of up-to-date information on a variety of procurement topics, including defense acquisition regulations, contract policies, program acquisition, cost and pricing, workforce management and strategic sourcing. From the site, you can keep up to date on DPAP news, subscribe to DFARS News and otherwise keep current on the Defense Federal Acquisition Regulation Supplement (DFARS) and related documents.

Defense Procurement & Acquisition Policy, Washington, DC. (703) 695-7145. [www.acq.osd.mil/dpap].

Special Feature

Military-Specific I/O

Military I/O Solutions Blend Functions and Fabrics

The struggle continues between legacy military I/O schemes like 1553 and new approaches like using Ethernet and a fabric I/O interconnect. Together 1 Gbit and 10 Gbit Ethernet, Extended 1553 and Fibre Channel are all jockeying for military mindshare.

Jeff Child
Editor-in-Chief

While the basic challenges of military I/O haven't changed—it's still all about linking the analog world of sensors, actuators, motors and so on, with the digital world of processing and control—the movement of where that analog to digital transition happens continues to move closer to the analog edge. That's driving demand to rethink how and where traditional military I/O interconnect schemes are used.

For its part, the long dominant MIL-STD-1553 has maintained its viability in a variety of military applications. While still an avionics bus at heart, the MIL-STD-1553 bus continues to play a role in a wide variety of systems such as tanks, ships, missiles and satellites. Several vendors continue to support 1553 with board-level solutions that provide 1553, often included with other functions. Among those vendors are AIM-USA, Aitech Defense Systems, Alpha Technology, Ballard Technology, Curtiss-Wright, Data Device Corp., Excalibur Systems, GE Fanuc and Kontron America.

Figure 1

Data Device Corp.'s BU-65578C MIL-STD-1553 PC/104-Plus card provides up to four dual redundant MIL-STD-1553 channels, five user-programmable digital discrete I/Os, selectable external or internal time-tag clock, and an IRIG-B time synchronization input.

With over 30 years now under its belt, 1553 remains an internationally accepted data bus standard for many military platforms. And for applications where data integrity and low latency are the priorities, 1553 is likely to remain the military interface of choice. Meanwhile Fibre Channel, Ethernet and Extended 1553 (E1553) top the list of possible upward migration paths from 1553.

1554 on PC/104

Earlier this year Parvus selected Data Device Corp.'s BU-65578C MIL-STD-1553 PC/104-Plus card for use in an application requiring a 1553 interface. The BU-65578C PC/104-Plus card (Figure 1) provides up to four dual redundant MIL-STD-1553 channels, five user-programmable digital discrete I/Os, selectable external or internal time-tag clock, and an IRIG-B time synchroniza-

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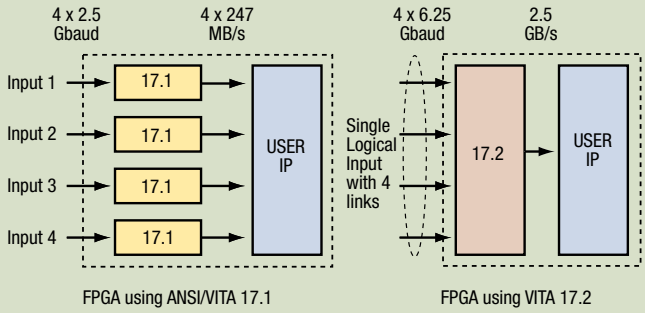
Serial FPDP Satisfies I/O Bandwidth Appetite

Most high-performance embedded computing systems in the military market have an appetite for high-speed data from sensors, often presented as one or more channels of analog data. In some cases, the sensor data is provided directly to the processing system. However, in other cases, the sensor data is converted to digital data by a smaller system near the sensor itself and then sent over one or more fiber optic links to the processing system. For these applications, Serial Front Panel Data Port (FPDP), or ANSI/VITA 17.1-2003, provides a simple point-to-point protocol with low overhead, high throughput and minimum latency.

When Serial FPDP was originally deployed, it was based on the fiber optic transceivers that were readily available at the time. The fastest version of Serial FPDP uses a bit rate of 2.5 Gbaud, providing of 247 Mbytes/s after 8B/10B encoding. As sensor technology improved, the sensor-to-processor interface often combined multiple Serial FPDP links to meet the ever increasing need for bandwidth. Although this approach provides the necessary throughput, it adds complexity at both ends of the link to manage splitting the data at the source and then aligning the resulting fiber optic streams at the destination. Because there is no standard method for doing this, link aggregation becomes an application-specific part of the problem.

The latest version of Serial FPDP, VITA 17.2, addresses these requirements in two ways. First, the choices for raw bit rates are expanded to include 3.125, 4.25, 5.0 and 6.25 Gbaud, allowing each link to operate up to 2.5x faster than before. Second, the standard now includes the capability to aggregate links in sets of 1x, 2x, 4x, 6x, 8x or 12x, allowing a single logical link to consist of multiple underlying physical links. The net result is that a stream of sensor data of up to 75 Gbaud (7.5 Gbytes/s) can now be considered a single Serial FPDP link.

Because most Serial FPDP implementations use FPGA technology to implement the protocol, support for the new standard can be added as an upgrade to existing products, typically without hardware redesign. For example, Tekmicro's JazzFiber V5 PMC/XMC module uses an FPGA-based architecture to implement four separate ANSI/VITA 17.1 links today with a total bit rate of 10 Gbaud, or just under 1 Gbyte/s (4 x 247 Mbyte/s) (see Figure). With a new 17.2 IP core installed as shown in the Figure, the module can support a single aggregated 17.2 link of 25 Gbaud or 2.5 Gbytes/s, using a Xilinx Virtex 5 FXT device to support links at 6.25 Gbits/s. By treating this as one logical link, downstream logic and complexity are both reduced, increasing the ultimate efficiency of moving data into the system for processing. --- by Andrew Reddig, President and CTO, TEK Microsystems.



Figure

Tekmicro's JazzFiber V5 PMC/XMC module uses an FPGA-based architecture to implement four separate ANSI/VITA 17.1 links today with a total bit rate of 10 Gbaud, or just under 1 Gbyte/s (4 x 247 Mbyte/s). With a new 17.2 IP core installed, the module can support a single aggregated 17.2 link of 25 Gbaud or 2.5 Gbytes/s, using a Xilinx Virtex 5 FXT device to support links at 6.25 Gbits/s.

tion input. The card has an intelligent hardware offload engine that dramatically reduces PCI bus and host CPU utilization, while storing 1553 Monitor data in a convenient and portable IRIG-106 Chapter 10 file format.

Parvus uses DDC's board in a U.S. Navy aircraft upgrade program and has also pre-qualified the card as an integration option for Parvus' DuraCOR 810 mission processor platform, which is being specified by prime contractors into a large number of U.S. military programs. Parvus has proven that this 1553 card successfully integrates into the system.

Thanks to the magic of today's level of semiconductor integration, multifunction mezzanine products have emerged and 1553 is part of that trend. This has enabled military system designers to blend a variety of I/O functions onto a single PMC. As an example along those lines, Aitech Defense Systems now offers a compact, multi-I/O PMC (Figure 2) that provides a variety of configuration options for the highest levels of flexibility in different I/O environments.

The low-power, single-width M705 features an unprecedented level of PMC density with up to five dual-channel, dual-redundant MIL-STD-1553B channels, 16 ARINC-429 receive channels and eight ARINC-429 transmit channels, up to six RS-232/422/485 serial channels and eight opto-isolated digital discrete input channels, all of which reduce the number of I/O cards required when developing subsystems. Additional board options include an ARINC 708 Weather Radar interface contained as VHDL within the large onboard FPGA.

The MIL-STD-1553 (STANAG 3838) channels support BC/RT/MT operation modes and offer 128 Kbytes (64K words) of dual-port RAM per channel. The discrete input channels serve as general-purpose I/O ports that connect to the GPIO FPGA, but are primarily used to externally assign the RT address to the MIL-STD-1553 channels. The PMC is available in the widest temperature range of -55° to +85°C (-67° to +185°F) and with software in rugged and military levels of ruggedization.

1553 in Rugged Box Systems

1553 is also prevalent in the emerging stand-alone rugged box category of systems. Kontron's latest offering along those lines is the Kontron MEC-PPC-AV1, a completely rugged Modular Embedded Computer (MEC) specifically targeted toward avionics applications. The Kontron MEC-PPC-AV1 is a low-cost 3U CompactPCI rugged subsystem designed to exceed requirements through its compact dimensions, low-power dissipation and real-time software with a very large I/O offering.

The Kontron MEC-PPC-AV1 is targeted toward the avionics market because of its ATR footprint dimensions, 28 VDC power supply, lightweight structure in aluminum, conduction-cooled dissipation, MIL-STD-1553 links, MIL-C-38999 connectors and a very low power consumption of less than 17W. The Kontron MEC-PPC-AV1 hosts a Kontron 3U CompactPCI Single-Slot PowerEngineC7 Embedded Computer, a low-power dissipation and high-performance processor board already embedded in major avionics programs. The PPC-AV1 offers a large range of I/Os such as Ethernet, general-purpose I/Os, serial lines and MIL-STD-1553 links thanks to the Kontron CPMC-1553-R PCI Mezzanine. The Kontron CPMC-1553-R is a redundant MIL-STD-1553B interface with two channels. The PMC module has a 32-bit, 33 MHz PCI interface and a parallel 8-bit TTL I/O port.

Figure 2

The M705 from Aitech Defense Systems is a compact, multi-I/O PMC that boasts up to five dual-channel, dual-redundant MIL-STD-1553B channels, 16 ARINC-429 receive channels and eight ARINC-429 transmit channels, up to six RS-232/422/485 serial channels and eight opto-isolated digital discrete input channels.

One tricky problem in the military I/O equation is the growing mismatch between compute density and I/O density. Next-generation UAV programs like the upgrades to the Global Hawk (Figure 3) involved replacing around 40 of its processor boards and replacing 30 of them with just a handful of FPGA-based cards. But while the move toward FPGA-based boards allowed Global Hawk payload designers to dramatically chop down the number of boards needed, they still face a

Figure 3

Recent upgrades to the Global Hawk UAV involved replacing 30 of its processor boards with just a handful of FPGA-based cards. But that consolidation creates a mismatch on the I/O side where a smaller set of boards must somehow accommodate the same amount of front-panel I/O.

nagging mismatch on the I/O side. Large UAVs like the Global Hawk are packed with a staggering amount and variety of I/O—everything from 1553 to RS-422 and RS-232. That means a smaller set of boards must somehow accommodate the same amount of front-panel I/O. System developers are looking at ways to leverage switch fabric solutions—or using Ethernet as a fabric—to ease that burden.

10 Gbit Ethernet as I/O Interconnect

Until recently, Ethernet's main role was as a control plane solution. Now, thanks in part to the emergence of rugged 10 Gbit Ethernet products, Ethernet is finally fast enough for data-plane use. Military system designers are now putting 10 Gbit Ethernet to work as a "fat pipe" to move data between subsystems. Military systems that need to pump data into a server farm, for example, for further processing and analysis are looking to 10 Gbit Ethernet as the interconnect linked directly into the server network.

Ethernet is being used as an interconnect fabric in compute-intensive applications like sonar, radar, or any application that networks sensor arrays together. This often means bridging to other protocols in electronic warfare (EW) or combat systems to move data from subsystem to subsystem or from box to box. Ethernet is being used to bring sensor data into other systems—as an alternative to other less common protocols like FPDP, Fibre Channel, or proprietary schemes. There's even a backplane standard for Ethernet released by the IEEE last year. The new standard, IEEE 802.3ap-2007, specifically targets backplane Ethernet applications. For its part, FPDP provides some unique qualities that give it a strong niche all its own. See the sidebar "Serial FPDP Satisfies I/O Bandwidth Appetite." ▮▮

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Power Transistor Advances Enhance Military Radar Designs

The pressure is on for military radar and avionics systems developers to boost performance while reducing system size. A new RF power transistor architecture helps smooth the way.

Daniel W. Ong, Product Manager
HVVi Semiconductors

Military avionics and radar design has seen profound changes over the past few decades. New multimode systems now allow radar to simultaneously track air and sea targets while continuously scanning an operational area. New signal processing techniques such as pulse compression increase resolution while maintaining range. Ground-based radar (GBR) systems operating in the 1.2 GHz to 1.4 GHz band offer better range and visibility than they ever have before.

Among the key driving forces behind these continual improvements in ground and aircraft-based primary and secondary radar systems has been developers' ability to improve power amplifier (PA) performance. Military radar and avionics systems developers are under constant pressure to maximize performance and efficiency while reducing component count, board and system footprint. Over the last several decades, the constant evolution of the RF power transistor, and its impact on PA design, has played a crucial role in this process. By continually improving RF transistor performance, military avionics and radar system designers have been able to deliver PAs capable of providing higher levels of power at higher efficiency and with higher linearity. Figure 1 shows a radar antenna system aboard the aircraft carrier USS Abraham Lincoln.

Figure 1

Through continuous improvements of RF transistor performance, radar designers have been able to get higher levels of power at higher efficiency and with higher linearity. Shown here is the SPS-49 air search radar antenna mounted atop the lattice mast aboard the nuclear-powered aircraft carrier USS Abraham Lincoln.

Constant Improvement

Back in the 1950s and 1960s, early development efforts of power transistors for RF applications centered on the use of Germanium. By the mid-1960s, however, military designers had largely migrated to bipolar components that offered high power in a cost-effective and familiar fabrication process. As performance demands increased in the 1970s, developers in the commercial markets moved to double-diffused Metal Oxide Semiconductors (DMOS). This new architecture used a vertical transistor design to support operating voltages from 28V to 50V at frequencies up to 500 MHz. Combining fast switching response, better thermal stability, higher input impedance

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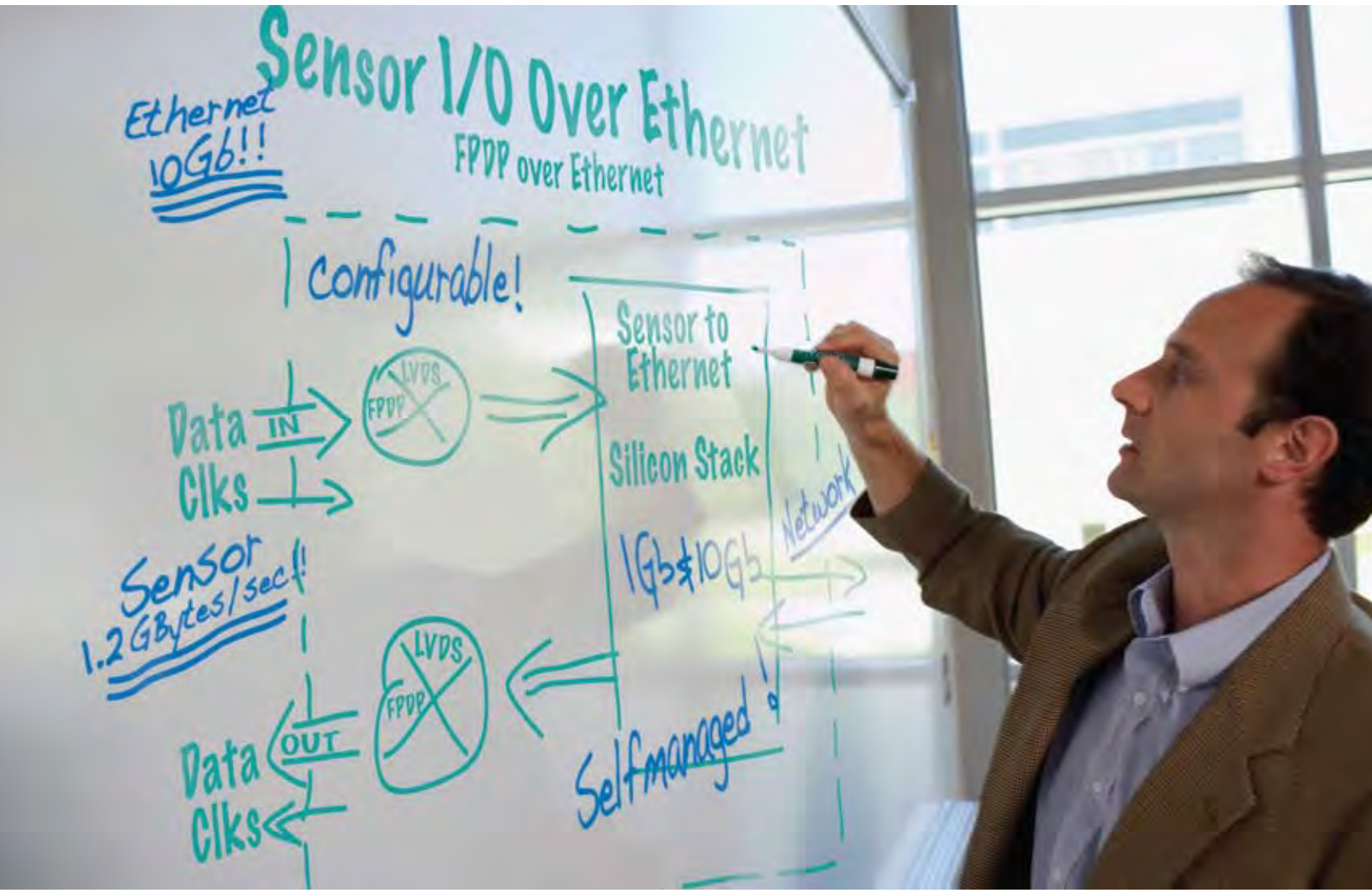

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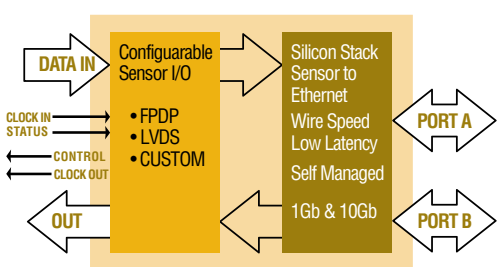

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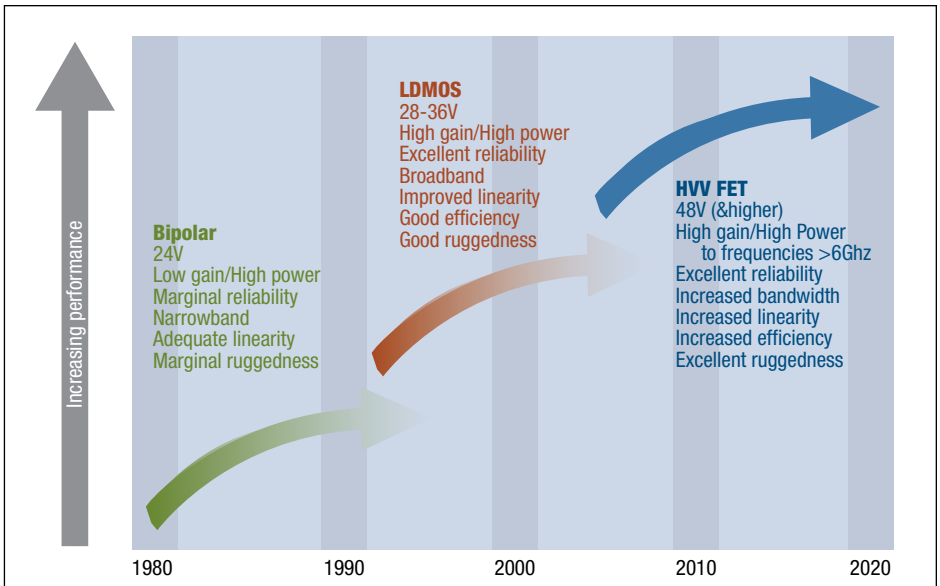

Figure 2

The history of power transistor development has progressed over the years from bipolar to LDMOS and now HVVFET.

and simpler circuit architecture, DMOS was widely adopted.

As commercial communications systems developers began building out the wireless infrastructure in the 1980s, escalating performance demands drove researchers to explore alternative strategies capable of meeting the higher power efficiencies required for PAs in base stations. Driving this effort were inherent limitations to the DMOS architecture. Wireless base station designers needed PAs capable of offering higher linearity to satisfy higher-order modulation schemes, greater average output power levels, broader operating bandwidths and lower system operating costs through higher power efficiency. To address this challenge, developers introduced the Lateral Double-diffused metal Oxide Semiconductor (LDMOS) power transistor. Figure 2 traces the history of power transistor development.

Despite these continual improvements in power transistor design, each architecture currently available brings with it significant limitations. Bipolar devices offer relatively high power density at high voltage levels, but with limited gain. Newer LDMOS alternatives promise improved gain and better efficiency, but with limited ruggedness. Power transistors fabricated in non-silicon technologies such as Gallium Nitride or Silicon Carbide deliver better performance through the technology's higher inherent electron mobility, at a significantly higher cost and with limited reliability.

Beyond Bipolar

Given the relatively long design cycles in the military market and the need for relatively high power and high reliability, most military designers have opted for bipolar devices to meet their design needs. Still, military designers are not immune to the same forces driving commercial radar designs. Developers of today's aircraft-mounted military radar systems are facing escalating pressure to reduce the size, weight and power consumption of their systems without sacrificing reliability or increasing cost. On the ground-based side, military system designers need solutions capable of delivering higher levels of output power without compromising efficiency or operational cost. In both cases, high reliability is a must. Clearly military system designers need a new approach to power transistor design that can be used to develop PAs with higher power density in smaller packages, while retaining high levels of ruggedness.

Recently, engineers at HVVi Semiconductors announced the first major advance in power transistor design since the development of LDMOS over 15 years ago. This

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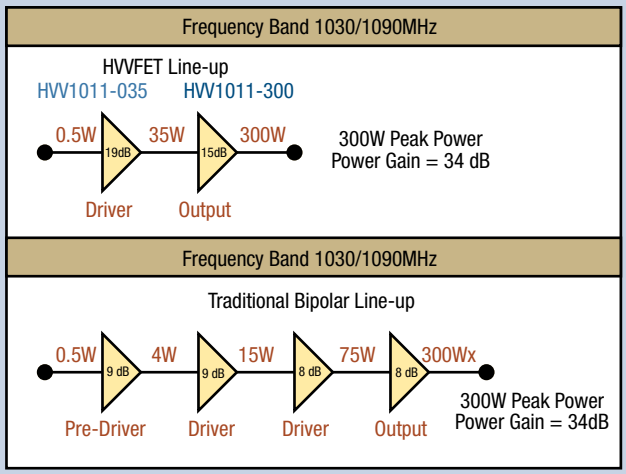

Figure 3

By offering more than twice the gain of comparable bipolar devices, power transistors using this new technology can dramatically reduce drive stage requirements. The Figure shown here compares a traditional bipolar transistor lineup to a lineup using the HVVFET. Shown here is a typical 300W solution for IFF applications in the 1030 to 1090 MHz band. Designers using traditional lower gain bipolar components would need to configure four stages of devices. Using easy-to-match 48V components based on the HVVFET architecture, designers can generate the same power using a 35W device offering 19 dB of gain to drive a 300W transistor providing 15 dB of gain.

By delivering 600W of power at 30 percent better system efficiency, a two-stage design reduces system power supply requirements and operating costs. The HVVFET-based design not only eliminates two driver stages, it also eliminates all of the capacitors in the RF interstage matching as well as a variety of supporting external components. PCB footprint requirements shrink by at least one-third and system costs drop proportionally.

new approach uses a High Voltage Vertical Field Effect Transistor (HVVFET) to support higher power levels through voltage. By reducing parasitic capacitances, this new topology is capable of 3X the frequency of LDMOS devices with a 30 percent boost in system power efficiency. Compared to the lateral transistor used in LDMOS, the vertical approach used in the HVVFET offers significantly higher power density, allowing component designers to deliver twice the power in the same package. Ultimately, designers believe this new architecture will support devices up to 150V and operation all the way up to 12.5 GHz.

Just as important to military system designers, this new architecture offers major advances in system ruggedness and reliability. The vertical structure of the HVVFET allows designers to develop transistors that deliver higher voltage while generating less heat. Heat is a major impediment to power amplifier performance and poses a primary threat to reliability. In a lateral power transistor like that used in LDMOS, the hottest part of the transistor is located approximately 100 microns from the heat sink. The heat dissipated by the device must pass through the entire thickness of the die.

Closer to the Heat Sink

In this new vertical design, the hottest point on the die is located less than 5 microns from the heat sink. That difference offers dramatic heat extraction advantages. Moreover, to better manage thermal performance, engineers at HVVi have bumped the die that rapidly dissipates the heat. As a result, power transistors built using this new architecture offer substantially better reliability. HVVi's first products, for example, are specified to withstand a VSWR of 20:1 at all phase angles under full rated output power or about 10x as high as bipolar devices and 25x the rating of LDMOS devices.

The HVVFET architecture's ability to scale to higher voltages offers unique

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advantages. The architecture depletes vertically into the substrate as voltage is applied to the drain. The architecture approaches planar breakdown in the vertical drain region and thereby stands off the maximum voltage with the minimum Rds(on). At the same time the architecture maximizes packing density while minimizing parasitic capacitance.

The architecture was designed so that performance characteristics improve as the device moves to higher operating voltages. For a higher voltage at a fixed RF power, the drain-source current of the device decreases. This allows power transistor designers to reduce die size and decrease parasitic capacitance per watt. Lower capacitance supports higher frequency operation and lower current improves system reliability.

System Implications

The most important advantages of this new architecture, however, come not at the individual device level, but at the system level. Figure 3 compares a traditional bipolar transistor lineup to a lineup using the HVVFET. One system advantage is that the lower current requirements associated with a higher voltage supply and lower thermal resistance improve system reliability and extend the system lifecycle. Moreover, since HVVFET transistors are specified to withstand a 20:1 VSWR at all phase angles under full rated output power, the new smaller design offers higher reliability. For airborne L-band applications such as these, fewer components also translate into less weight. Moreover, the technology's significantly higher VSWR rating may allow designers to eliminate the use of isolators and, in the process, further reduce system weight and cost. Finally, a simpler design with fewer components translates into simpler system architecture and the expenditure of fewer design resources.

Similar advantages are achievable in ground-based radar applications. Figure 4 shows an HVVFET-based configuration for L-band pulsed radar applications in the 1.2 to 1.4 GHz frequency band. In the HVVFET configuration, a 25W device with 18 dB of gain drives a pair of 100W transistor providing 19 dB of gain. The lineup provides 200W of power at over 47% efficiency. Again, by reducing amplification stages, the designer earns major improvements in system footprint, cost and reliability.

Constant Trade-Off

Power amplifier design is a constant trade-off among performance attributes. Historically, designers have had to balance improvements in power output or gain against limitations in linearity or efficiency. The continual evolution of silicon RF power transistors is gradually undermining that perception however. With each new generation developers have been able to tweak architectures to meet new performance requirements. The latest development in RF power transistors with the HVVFET architecture promises to deliver higher power density, efficiency and reliability levels to next-generation military radar and avionics system. ▮▮

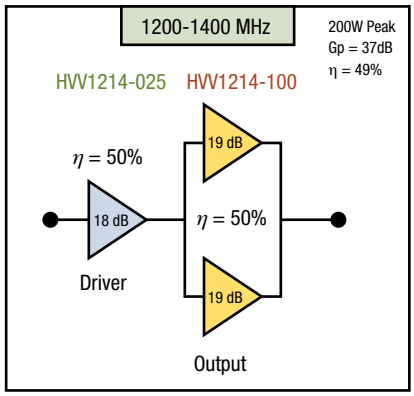

Figure 4

Shown here is an HVVFET-based configuration for L-band pulsed radar applications in the 1.2 to 1.4 GHz frequency band.

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Tech Recon

Taming System Complexity

Multiprocessor-Specific Tools Enable Efficient Real-Time Development

Complex applications like radar are being built with larger numbers of processors. System designers are faced with repetitive tasks just to get started. Tools are emerging to smooth such hurdles.

Darian Wong, Product Marketing Manager, System Software Tools
Curtiss-Wright Controls Embedded Computing

Today there are numerous software development tool choices for aerospace and defense system programmers developing embedded real-time applications on single processor systems. But once you leave the single processor paradigm and attempt to develop multiprocessor real-time applications, one finds that existing tools don't easily scale. And the problem becomes commensurately more difficult with an increasing number of processors in the system. For military applications such as radars and signal intelligence, multiprocessing systems are essential, providing the performance required to process the source signals in real time.

As radar systems become increasingly powerful in order to track a greater number of targets, multiprocessor systems are being built with larger numbers of processors (Figure 1). Unfortunately, what is simple and fast for a uniprocessor system can become laborious and error-prone when working with a multiprocessor system comprised of 16, 64 or even hundreds of processors. Today, multiprocessor system programmers are confronted with the need to do numerous repetitive tasks just to get their system up and running. A better approach is a tool for multiprocessor real-time development that understands the unique challenges entailed.

Figure 1

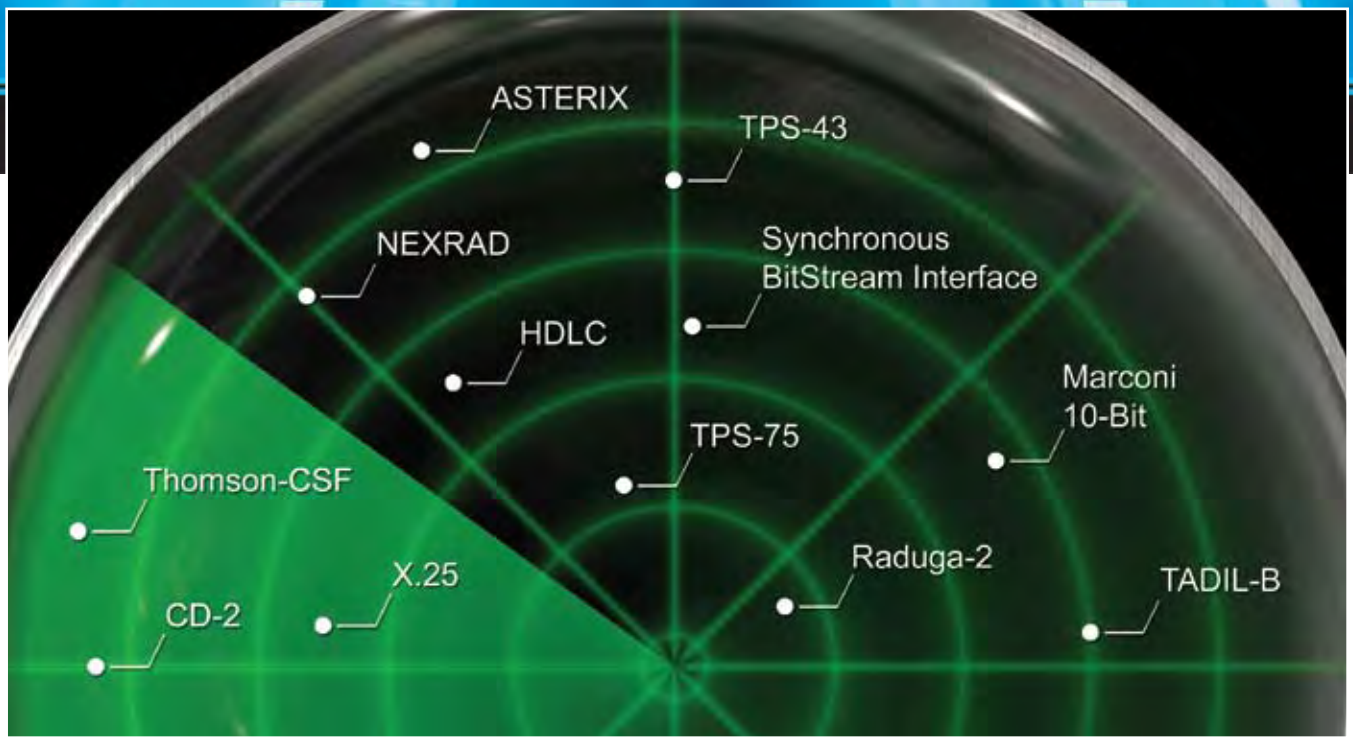
Typical embedded multiprocessor system for use in aerospace and defense signal processing applications.

Multiprocessor Problems

Today's single processor real-time tools are designed for use where the programmer is developing with one single board computer and one processor. In a typical cross-hosted embedded software environment, the frequently recurring cycle of edit/compile/load/debug involves a number of manual steps either with traditional command line control or with graphical Integrated Development Environments (IDE) such as Eclipse. The problem arises with multiprocessor systems. For example, with a 64 processor multicomputer one would have to repeat the same manual steps 64 times before the system could be booted and tested. This process is very cumbersome and today's tools don't scale to address the problem. Worse, for every additional processor, one adds one more step. The pitfalls are significant. One entry mistake means having to begin again from the very first step. Without a tool that understands multiprocessor systems, the process is rife with potential human error, time-consuming and labor-intensive

Hierarchical Approach

A better approach would enable the programmer to treat the system at a hierarchical level. It is common in multiprocessor systems for identical code to be running on groups of processors. A multiprocessor-aware tool would allow the developer to define groups of processors that run the same code. Once these mul-



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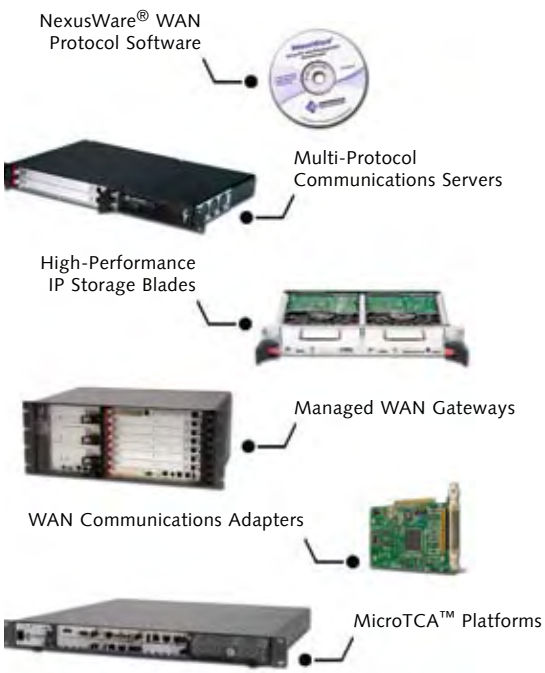

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tiple groups that span the entire system have been defined, it should be possible to operate on all the processors within that group. For example, one could define a signal processing group that includes all the nodes of a particular quad processor DSP board, and all those processors are running the same kernel and the same application. With a single key stroke it would be possible to download the application not only to one processor but to all the processors within that group. After, similar operations can be performed on the other groups that have been defined to comprise the system.

Even better, a multiprocessor system would provide a GUI for an icon-based representation of the system as opposed to requiring that the programmer write scripts. Providing different views of the system, for example, chassis level, card level, component level and group level, would significantly ease and speed the process of working with the system.

Another area of multiprocessor system development not well met by today's single processor tools is debugging. A popular tool for single processor real-time debugging is System Viewer from Wind River. System Viewer provides time stamped event analysis of what happens within the application. There are standard events that are related to OS activities such as task, context switches, interrupts, task delays and network activity. In addition, it enables users to instrument their own code to add user-level events within their own application. This enables, for example, notification of when an FFT is begun or completed and when the results of that FFT are transferred to another processor in a pipeline operation. For multiprocessor systems, the difficulty is getting the information time-aligned, across multiple processors (Figure 2). The challenge is to find a way to ensure that your timestamps are common across multiple processors. Then, by hand, you would need to correlate that timing information into some method of analysis that showed when events occur on one processor versus another. Today this would typically be in a non-visual fashion, and would become increasingly difficult when scaled to larger and larger systems.

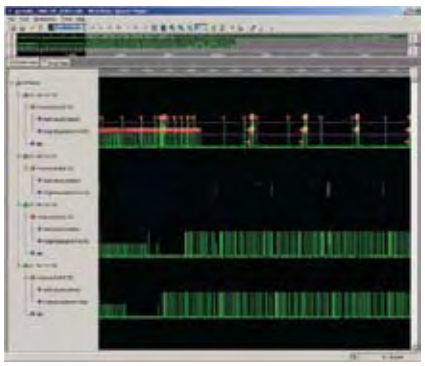

Figure 2

Curtiss-Wright's Continuum Insights enhance Wind River's System Viewer for use with multiprocessor systems.

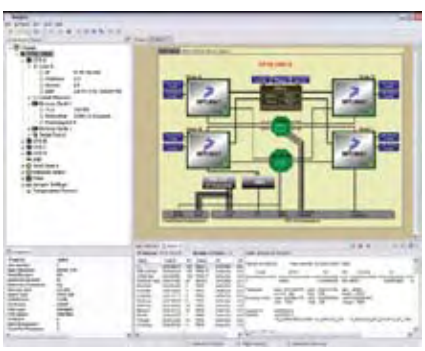

Figure 3

The Continuum Insights System Monitoring tool displays a system-, board-, or component-level graphical view of system health and status.

Bringing it All Together

A commonly used development method to gain visibility into the state of software execution is to log messages to a console, aka *printf*. This approach is time-proven, but how does one scale this technique to a system of 64 processors? Imagine 64 serial cables and 64 instances of a terminal emulation program running on the development host. This is clearly not feasible. What is needed is a tool that allows the consolidation of all of the processor log messages with a means to organize and delineate by processor and time in space and time the different messages.

A source-level debugger is one of the tools used to determine the cause of faulty behavior of a program. The debugger allows a programmer to halt execution on the basis of location or the state of variables in a system and then proceed with single stepping techniques to identify problem areas in the code. Every programmer uses one.

The traditional source-level debugger is severely lacking in functionality for working with a multiprocessor system. For example, what if you want to know what is happening on CPU #2, at the moment in time when CPU #1 hits a breakpoint? What if the continuing operation of CPU #2 will interfere with the state of CPU #1 while it is halted? A traditional source debugger has no facility to work past the confines of a single processor.

Capturing Entire System State

A multiprocessor system calls for a scaled-up source-level debugger that can support breakpoints in multiple processors whereby the entire system, or selected processors, can be halted and thus allow examination of the state of the entire system at the point of interest.

To solve a number of these multiprocessor real-time system development problems, Curtiss-Wright has developed a tool called Continuum Insights. Designed to support systems ranging from a few to hundreds of processors/cores, Continuum Insights addresses the described shortcomings of uni-processor development/debug tool chains. Insights is based on the Eclipse Development Framework, and provides an extensive suite of capability to work with large multiprocessor systems (Figure 3). Developers can dramatically improve their productivity by using Insight's functionality to download, analyze, debug and monitor a multiprocessor system logically organized into groups of processors according to the way that makes sense to the programmer. ▮▮

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Tech Recon

Taming System Complexity

From Defense Mission to Development Workflow: Making the Link

Today's most complex, Net-centric military programs require a formidable amount of workflow automation and organization. Standards, change control and a "systems" perspective are all key to making that happen.

Adrian Whitfield, Director, Aerospace and Defense Industry Marketing
Telelogic, An IBM Company

In May of 2003 the Department of Defense outlined its vision of a net-centric environment and the data goals for achieving that vision as "… the realization of a networked environment, including infrastructure, systems, processes, and people, that enables a completely different approach to war-fighting and business operations." Today that vision is becoming a reality. Equally real are the challenges faced by defense industry professionals tasked with evolving and developing the systems and software required in a net-centric environment. One area that is receiving attention is support for a more tightly integrated and efficient workflow, starting with a "system of systems" enterprise architecture and drilling down into project-specific architectures, including systems engineering and software development. The Army's Future Combat Systems program is an excellent example of a complex military program requiring that system of systems approach (Figure 1).

Figure 1

The Army's Future Combat Systems program is an excellent example of a complex military program requiring that "system of systems" approach to software development. The FCS Network is a layered system of computers and software, radios and sensors all interconnected with each variant in the FCS Brigade Combat Team.

Adopting more efficient and streamlined workflows presents an opportunity for both defense agencies and integrators to solve today's critical defense challenges. Teams can tie development of embedded software and systems directly to program mission, capabilities and goals. This integrated approach allows defense organizations to use modeling and architecture technology as a platform to streamline the manual tasks associated with development and better focus their efforts on the intellectual aspects of development.

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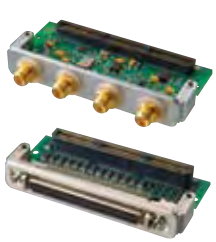

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Figure 2

Tools can help optimize workflow from high-level missions, strategies and operations in an enterprise architecture to the detailed systems engineering and embedded software views that are part of software development.

Three Critical Areas

The trend toward tightly integrated workflows is tied to three critical areas. First is adopting a formal workflow that begins with a system of systems enterprise architecture (EA) and extends through system engineering and software development, including tasks at the embedded level. Second is establishing standards compliance to meet net-centric, Department of Defense Architecture Framework (DoDAF), UK's Department of Ministry Architecture Framework (MODAF) and NATO Architectural Framework (NAF) requirements. And the third area: adopting a formal change control and governance program for EA and software development programs. By meeting these targets, a defense organization can overcome many of their most difficult development challenges.

Where to Begin

To successfully develop defense applications in a global defense environment, organizations should try to make the best use of technology to quickly come to terms with change. For example, development and architecture teams can look at ways to use technology to easily work together on long-term projects across multiple time zones. By using DoDAF, MODAF, NATO and net-centric defense standards, they can more quickly develop both IT and embedded systems that meet net-centric requirements. In addition, teams can use tools that support starting at a system of systems enterprise architecture all the way through system engineering and embedded software.

Today's technology is designed to help defense agencies and integrators to focus their efforts where they add the most value—the intellectual aspects of development, not the execution of technical tasks. Teams can adopt technologies that ensure traceability of requirements, design attributes and other implementation artifacts throughout the entire development process.

The first step is examining the benefits of an architecture-through-deployment lifecycle that streamlines the implementation of defense architecture and modeling initiatives. This approach extends the powerful model driven development (MDD) environment to architects, engineers and developers.

A seamless, model-based workflow throughout the architecture-to-system engineering/embedded software lifecycle provides a bi-directional link between mission and goals and systems development. Defense architectural standards then can be incorporated throughout the project to provide guidance, and a common platform for easily sharing information across dispersed teams can be deployed. Architecture and development environments are more tightly integrated, resulting in a rapid response to changing defense environment dynamics. Resource integration across architecture and IT disciplines helps defense organizations act more efficiently and effectively.

To accomplish this, many organizations are adopting a system of systems approach that uses an EA-to-system engineering/embedded software process. This helps development and architecture teams to op-

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Figure 3

Defense organizations often need to support the various views offered by architecture framework standards such as DoDAF and MODAF. Tools such as Telelogic Rhapsody can now streamline the model-driven development process.

timize their workflows, moving from high-level missions, strategies and operations to detailed systems and real-time embedded software development. Stakeholders can transfer model information between two repositories, closely aligning embedded and real-time systems development with defense missions and strategies.

Today's MDD solutions support data synchronization between traditional EA and embedded development products. This supports effective management of different workflows across an organization and provides an optimal workflow for integrators who can work from the highest-level operational concepts and drill down to granular technical systems and embedded software development. As a result, development teams can more easily understand the context of systems engineering, from the system of systems level to system, subsystem, and even down to the component level.

Moving from a system of systems approach through an EA-through-system engineering and embedded software development process allows engineers and developers to share and synchronize information across modeling solutions, avoiding duplication errors while improving accuracy. Development time and cost are reduced and tool usage is optimized. Teams are able to use the right tool for the job at hand. In addition, engineers can take advantage of industry standards such as the Systems Modeling Language (SysML) for system engineering or Unified Modeling Language (UML) for software engineering in their embedded designs. Requirements Management and change control solutions can also be added to ensure traceability is maintained between the EA and embedded development products. Figure 2 shows a UAV example project where model information is moved between a high-level concept to a detailed design.

Standards Compliance

In the past, the defense industry has been focused on meeting DoDAF, MODAF and NATO architecture standards. Today, however, there is a new emerging standard: net-centric operations. The Department of Defense (DoD) mandates that all advanced weapons platforms, sensor systems, and command and control centers support net-centric operations, and that warfare must be "net-enabled." The impact of this new standard on defense organizations is that defense applications must be designed as part of a broader landscape that emphasizes the "ability to share information when it is needed, where it is needed, and with those who need it." The directive includes all aspects of EA and software development, including IT and embedded systems. Thus, architecture and development teams are required to take into account all governance and compliance requirements.

In order to meet key net-centric compliance requirements, an organization must be able to capture detailed net-centric specific information within a model, such as detailed interface descriptions. This requirement represents a paradigm switch for many defense integrators. The net-centric standard requires an embedded component or real-time constraint. As a result, complex sensors or war fighting nodes—aircraft, communications, vehicles, radar, and so on—within the theatre of operations and the technical applications that communicate with the embedded systems—complex control systems—must all provide net-centric support for an EA to be compliant.

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SOA's Net-Centric Role

The net-centric operations standard further revolutionizes the systems engineering and software development/embedded systems process by introducing the Service Oriented Architecture (SOA) concept to the development lifecycle. SOA is one of the key enabling technologies to meet the net-centric standards. SOA support for embedded systems development allows developers to define and visualize SOA interfaces using an SOA profile, with further support for importing and generating Web Service Description Language (WSDL) files.

In addition, domain-specific profiles within today's MDD environments allow for intuitive specification and services usage, all in a platform-independent manner. The modeling environment offers an organization many advantages. WSDL files can be generated out of the platform-independent model. Powerful model execution and simulation capabilities and advanced testing and production-quality code generation enable developers and engineers to easily support a SOA approach for building net-centric operations and warfare applications.

For non-net-centric defense applications that still need to comply with industry architecture standards such as MODAF, DoDAF and NATO, a model-driven approach is paramount. As part of an MDD approach, a centralized model repository where architecture product deliverables can be quickly produced is essential. Often information only needs to be entered once, and then several architecture product deliverables or views can be derived from a single information repository. Being able to take advantage of model execution and simulation to explore and test the design architecture before detailed implementation, can save valuable project dollars and later testing time. Figure 3 shows how Telelogic Rhapsody can streamline the model-driven development process and support the various views offered by architecture framework standards such as DoDAF and MODAF.

Governance and Change Control

The final area to be addressed is to implement a formal change control and governance program that provides oversight for EA and software development programs and related initiatives including DoDAF, MODAF and net-centric operations. Software for tracking, change requests and workflow management across a program helps address the complexity associated with defense EA and development programs.

Change management software tracks the architectural model building process, providing visibility over change requests and a formal way to analyze their impact on IT and business functions. Answers to questions such as "Who is responsible for this change?" or "Why was this changed?" and "What is the impact of this change?" can be generated and discussed.

The benefits to embracing a formal approach to EA governance extends to other critical areas. Agencies and con-

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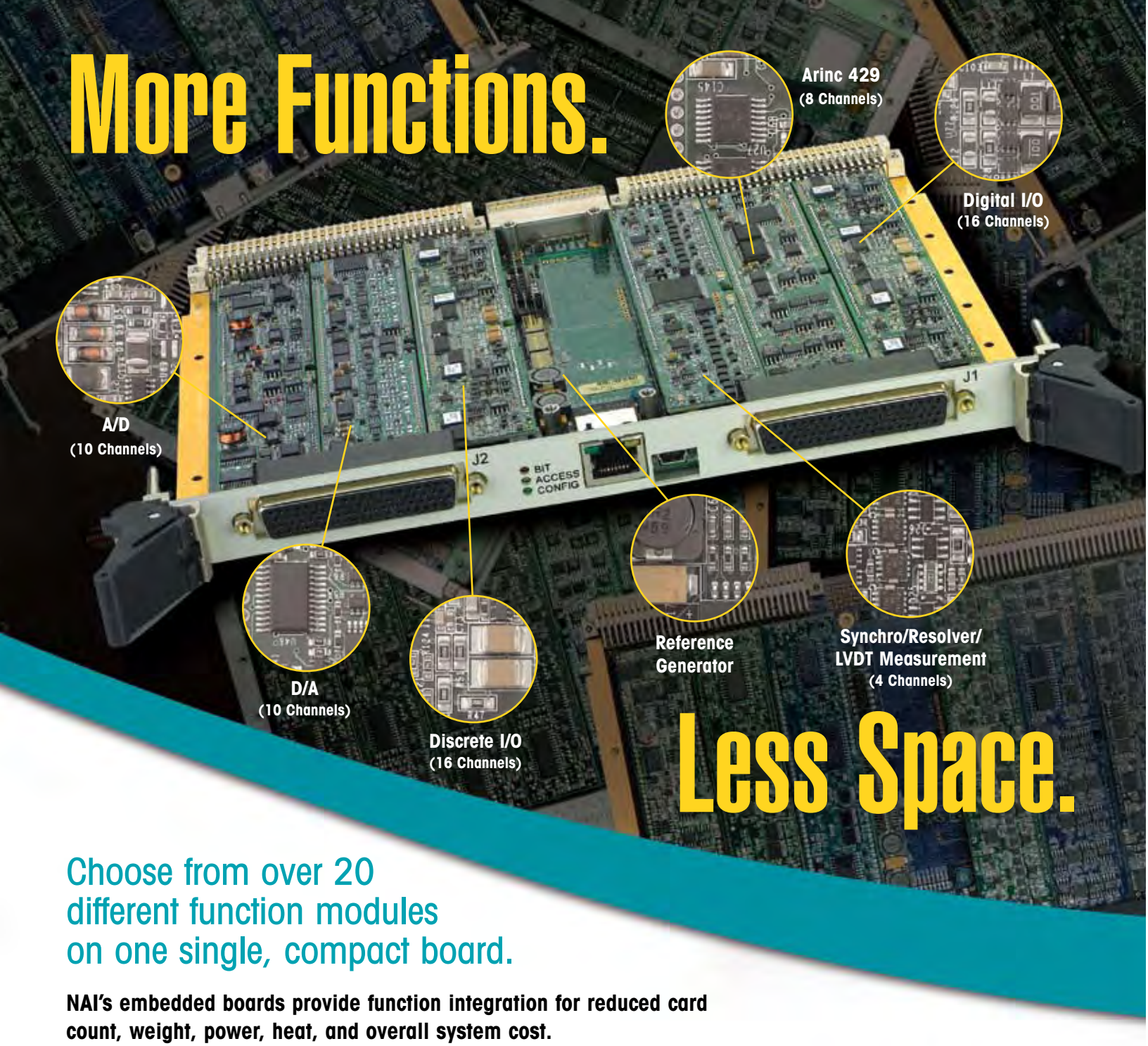

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tractors can effectively facilitate how they work together by synchronizing the work of multiple teams and establishing a formal, well-understood governance and compliance process. By simplifying the projects and changes over time, agencies can better manage project customization. Parameters can be set for project security, project status and change reporting. A trail of changes can be archived and referenced in the future, effectively creating a "living" document that can be used to prove compliance or develop new designs going forward.

The future belongs to those defense organizations that can meet the many challenges of moving to a net-centric environment. By streamlining their development process to get an architecture-through-systems engineering/embedded software lifecycle, organizations can better address the complexity of these programs and improve communication across all stakeholders. By embracing a new approach that adopts an integrated workflow that seamlessly moves from the high level to the technical, organizations capitalize on the net-centric opportunity.

Three Keys to Success

Organizations that undertake actions in three critical areas will see the best results: Adoption of a tightly integrated, architecture-to-development workflow; faster adoption of defense architecture standards; and a formal approach for change control with EA program governance, will provide a solid platform for handling change. Defense organizations that optimize their use of technology and leverage the right combination of solutions for each job, will find numerous benefits in areas of communication, costs and time. The additional functionality that an integrated MDD/EA/SOA solution offers, such as integrated requirements management and IT systems development, will further streamline the development process and help boost quality and accuracy.

With resource integration across architecture and IT disciplines, defense organizations can more easily deploy a seamless model-based workflow throughout the architecture-to-development lifecycle and provide a bi-directional link between missions, goals and IT/systems development. A lifecycle management solution that supports EA-through-systems engineering and embedded systems development delivers a platform for enabling defense agencies and integrators to focus on what they do best: contributing their intellectual assets while streamlining the underlying technical process.

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		CMA157886PX1400HR	CMX158886PX1400HR	CMD158886PX1400HR	CMX158886PX1400HR-BRG	CMD158886PX1400HR-BRG	CME147786CX400HR	CME147786CX650HR	CML147786CX400HR	CML147786CX650HR	CMX147786CX400HR	CMX147786CX650HR	CME136686LX500HR	CME137686LX500HR
Expansion Bus	PC/104 ISA Bus	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI-104 PCI Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓
	PCI Bus Masters	4	4	4	4	4	4	4	4	4	4	4		4
	APIC (add'l PCI interrupts)	9	9	9	9	9	9	9	9	9	9	9		
CPU and BIOS	CPU Max Clock Rate (MHz)	1400	1400	1400	1400	1400	400	650	400	650	400	650	500	500
	L2 Cache (KB)	2048	2048	2048	2048	2048	256	256	256	256	256	256	128	128
	Intel SpeedStep Technology	✓	✓	✓	✓	✓								
	ACPI Power Mgmt	2.0	2.0	2.0	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0		
	Max Onboard DRAM (MB)	512	1024	1024	1024	1024	512	512	512	512	512	512	512	512
	RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	RTD Quick Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Peripherals	Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	ATA/IDE Disk Chip (MB)	4096	4096	4096	4096	4096	4096	4096	4096	4096	4096	4096	4096	4096
	Audio		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Analog Video	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA
	Digital Video	LVDS	LVDS	LVDS	LVDS	LVDS			TTL	TTL	LVDS	LVDS	LVDS	
	AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O	**RS-232/422/485 Ports**	4	4	2	4	2	2	2	2	2	2	2	2	2
	USB Ports	4	2	4	2	4	2	2	2	2	2	2	2	2
	10/100Base-T Ethernet	1	1	1	1	1	1	1	1	1	1	1	2	1
	ECP Parallel Port		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	aDIO (Advanced Digital I/O)	14	18	18	36	36	18	18	18	18	18	18	18	18
	multiPort (aDIO, ECP, FDC)		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SW	ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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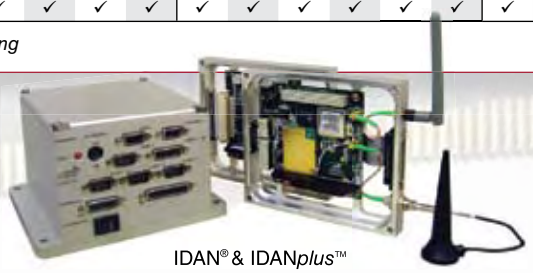

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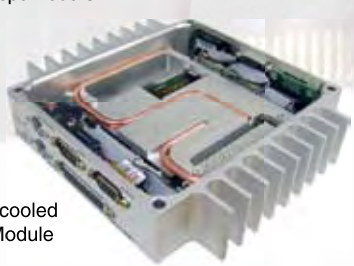

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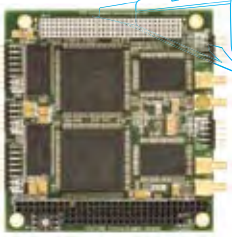

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Bus	Active Bus	PCI	PCI	ISA	ISA	PCI	PCI	PCI	PCIe	ISA	ISA	ISA	PCI	PCI	PCIe	PCI
	Passthrough Bus	ISA				ISA	ISA		PCI				ISA		PCI	ISA
	DMA or PCI Bus Master	✓	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓	✓
	McBSP Serial Ports	✓	✓			✓	✓	✓	✓							
Analog Input	Single-Ended Inputs	16	16	16	16	16	16	16	16							
	Differential Inputs	8	8	8	8	8	8	8	8							
	Max Throughput (KHz)	1250	1250	500	100	1250	500	500	500							
	Resolution (bits)	12	12	12	16	12	16	16	16							
	Input Ranges/Gains	3/7	3/7	3/4	1/4	3/6	3/3	3/3	3/3							
	Autonomous Calibration	✓	✓													
	Data Marker Inputs	3	3	3		3										
Conversions	**Channel-Gain Table**	1K	1K	1K	1K	1K	1K	1K	1K							
	Scan/Burst/Multi-Burst	✓	✓	✓	✓	✓	✓	✓	✓							
	A/D FIFO Buffer	8K	8K	8K	8K	8K	8K	8K	8K							
	Sample Counter	✓	✓	✓	✓	✓	✓	✓	✓							
	SyncBus	✓	✓			✓	✓	✓	✓							
Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	16	48	18/9	64	48	48	48	48
	Bit Programmable I/O	8	8	8	8	8	8	8	8	24	6/0		48	48	48	✓‡
	Advanced Interrupts	2	2	2	2	2	2	2	2	2			2	2	2	✓‡
	Input FIFO Buffer	8K	8K	8K	8K	8K	8K	8K	8K							
	Versatile Memory Buffer												4M	4M	4M	8MB
	Opto-Isolated Inputs											48				
	Opto-Isolated Outputs											16				
	User Timer/Counters	3	3	2	2	3	3	3	3	3	3		10	10	10	6
	External Trigger	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓‡
	Incr. Encoders/PWMs										3/9		4/8	4/8	4/8	✓‡
Analog Out	Analog Outputs	2	2	2	2	2	2	2	2							
	Max Throughput (KHz)	200	200	200	100	200	100	100	100							
	Resolution (bits)	12	12	12	16	12	16	16	16							
	Output Ranges	4	4	3	1	4	5	5	5							
	D/A FIFO Buffer	8K	8K			8K	8K	8K	8K							

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Team Effort Is Central Focus in DO-254 Compliance

Military and aerospace engineers and engineering managers shouldn't "go it alone" when embarking on the DO-254 process. What's needed is an ecosystem of partners that offers a range of DO-254 certifiable solutions.

J. Ryan Kenny, Technical Marketing Manager
Karl-Heinz Gatterer, Military and Aerospace Marketing Manager Europe
Altera

For most defense engineers, the first time they hear about the DO-254 Design Assurance Standard is in a request from their customer beginning with the words "Thou shall comply with DO-254." This leaves many engineers and engineering managers unsure of how to get started on the DO-254 process. As they soon find out, there is no "one-stop-shop" approach to finding a vendor who provides all the necessary training, documentation, verification and IP/hardware for their project. DO-254 compliance requires an ecosystem of partners that offers a range of DO-254 certifiable solutions.

The History of DO-254

As more software and embedded code began to see usage in safety-critical and avionics applications, the Radio Technical Commission for Aeronautics developed the RTCA/DO-178B: Software Considerations in Airborne Systems and Equipment Certification. With the increasing use of high-density circuits and programmable logic in safety-critical and avionics equipment, the DO-254 body was formed in 2000 to offer equivalent hardware design guidelines and certifications for hardware engineering. While initially developed for the European and U.S. civil aviation markets, DO-254 guidelines are now spreading into defense markets. The guidance requires all airborne systems featuring complex electronic hardware, such as FPGAs, PLDs and ASICs, to comply with the standard.

Figure 1

The three major components of a DO-254 FPGA Design include certifiable IP cores, a documented design verification flow, and final process documentation and training for design personnel.

The Design Assurance Guidelines for DO-254 break down the safety-assurance requirements of each design element of a military or avionics system based on its impact on aircraft mission and survivability in the case of failure. There are five levels of compliance, A-E, which depend on the effect a failure of the hardware will have on the operation of the aircraft (Table 1). Level A is the most stringent, defined as "catastrophic," while a failure of level E hardware will not impact the safety of the aircraft. The DO-254 Design Assurance Standard generally focuses on the first four design assurance levels.

The terminology used as it relates to DO-254 is an important part of the compliance process, as it helps identify where documentation and verification effort is required, versus where precedent and experience may be sufficient. For example:

- ***Certified***: an entire system is certified and components may have different certification levels
- ***Certifiable***: component within a system achieving its highest certification status prior to certifying it within the system

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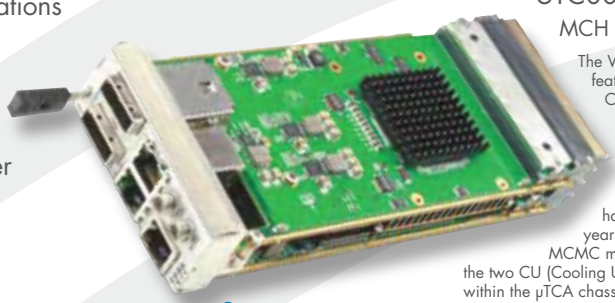

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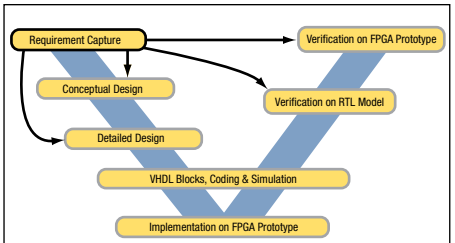

Figure 2

DO-254 guidance and consultation offer several different approaches to a DO-254 design flow for military and avionics hardware. The V-cycle shown here illustrates the typical certification process based on identification and validation of the requirements and their life cycle through the V-cycle certification process.

- ***Qualified***: certification of a tool, which itself does not have safety requirements

Cost Risks in DO-254 Certification

There are many managerial concerns about the impact of DO-254 certification on the cost efficiency of design organizations, and on the end equipment price of avionics and military equipment subject to certification. This manifests in cost risk and uncertainty in development schedules, inefficiency where DO-254 documentation practices are not yet in place, and inability to scope projects where certification procedures are not clear. Experienced partners and consultants are the best bulwark against this cost and efficiency risk. It is essential to work closely with experts, such as a DER (Design Engineering Representative) in North America or certification expert consultants in Europe, who will help prepare certification audits. These experts act as an interface between the system provider and the FAA or the European Aviation Safety Agency (EASA).

Expected DO-254 cost impacts are highly variable. The text Avionics Certification offers several cost rules of thumb for DO-178B software certifications, starting with a baseline cost at DAL level E, and up to 65 percent program cost impact at design assurance level A. For DO-254, a survey performed by the European "DO-254 Users Group" provides the following estimated cost impacts (Table 2). These include first an estimate of additional man-hours of effort for the DO-254 activity, and then an overall cost impact for the program that reflects changes to oversight, review cycles and configuration dependencies.

DO-254 Components and Work Flow

Some of the requirements of a DO-254 work flow may be met by the internal Capability Maturity Model Integration (CMMI) capabilities of a defense organization. These processes ensure that design certification and verification plans are developed in the right order in a hardware work flow. Even with these processes in place, however, much additional work

DO-254 Design Assurance Levels

Level	Description	System Example
A	Failure will cause or contribute to a catastrophic failure of the aircraft	Mechanical Guidance, Aircraft Control, Life Support, Power, Primary Flight Systems, Sensors, Actuators
B	Failure will cause or contribute to a hazardous/ severe failure condition	Flight Displays, Indicators, Auxiliary Controls
C	Failure will cause or contribute to a major failure condition	Navigation Displays, Aircraft Communications
D	Failure will cause or contribute to a minor failure condition	Internal Mechanical, Crew Equipment
E	Failure will have no effect on the aircraft or on pilot workload	Passenger Equipment

Table 1

Described here are five levels of DO-254 compliance, A-E, which depend on the effect a failure of the hardware will have on the operation of the aircraft.

Level	Effort to Reach Certification Level	Change to Existing Baseline
A	< 50 MM (Man Month)	From x1.4 to x1.6 extra work
B	< 50 MM	From x1.2 to x1.4 extra work
C	< 5 MM	1
D	Already reached	---
E	Already reached	---

Table 2

These results from a survey performed by the European "DO-254 Users Group" provide the estimated cost impacts. These include first an estimate of additional man-hours of effort for the DO-254 activity, and then an overall cost impact for the program that reflects changes to oversight, review cycles and configuration dependencies.

is needed to meet the expectations of the aviation certification guidance.

The establishment of the DO-254 User Groups and the formation of DO-254 partner networks have helped alleviate much of the pain and costs associated with achieving DO-254 certification. DO-254 partner networks feature representatives from each of the major DO-254 segments, including certifiable IP cores, a documented design verification flow, final process documentation and training for design personnel (Figure 1).

The DO-254 Design Assurance Standard refers to about 30 different items, four of which are submitted to the certification authority to obtain DO-254 certification. These include the Plan for Hardware Aspect of Certification (PHAC), a Hardware Design Plan and Validation, a Verification Plan and the Hardware Accomplishment Summary. The higher the system's design assurance level, the more complex the system, the more guidance the designer must follow, and thus the greater the development process costs. The PHAC, which is a design assurance approach document, is required for certification for all levels. The PHAC is one of the most important documents, in that insufficient planning or coverage in the document could delay the program or increase the cost.

Several Different Approaches

In order to address each of these individual components, DO-254 guidance and consultation offer several different approaches to a DO-254 design flow for military and avionics hardware. The V-cycle in Figure 2 shows the typical certification process based on identification and validation of the requirements, and their life cycle through the process. The traceability of the requirements from the system to their verification has to be established and demonstrated to the certification authority. Each of the partners in a DO-254 certification network has a different role in the success of DO-254 certification requirements. At level A and B, it is also essential to demonstrate the team independence between the development and the validation and verification phases.

The DO-254 process is sometimes referred to as a chain, where the entire system is only as strong as its weakest link. This metaphor refers to both the process flow and the DO-254 teaming arrangement. In a process flow, each tool and certification step needs equal qualification standards, resources and scrutiny from certifying officials. When referring to a DO-254 partnership network, this refers to the confidence certifying officials have in a teaming arrangement with experienced and capable DO-254 providers. The roles of different DO-254 providers in a network are described below.

Planning: One of the cardinal rules of DO-254 compliance is that planning precedes development. Subsequently, designers then have the burden of showing that this compliance plan was followed. The compliance plan is where potential partnerships are investigated and pursued, and where certifying officials begin when assessing the completeness of a DO-254 certification process. Planning may consist of several distinct documents for certification, quality assurance, configuration management, development and verification (described earlier).

Education and Process Support: An important part of controlling the cost risks in DO-254 certification is the education of engineering and quality assurance staff, and in identifying best practices in DO-254 certification. Geensys in Europe and HighRely in North America offer consulting, documentation support and training.

Verification Methods and Tools: Verification is an area of growing concern to many companies designing modern avionics. In many cases, old verification methods have not kept pace with complexity on the design side, resulting in serious schedule delays and/or quality issues. The purpose of the DO-254 standard is design assurance, and this means fully verifying that a design performs its intended function. Over the last decade, the design automation industry has seen rapid advancements in the area of functional verification to address the challenges of testing complex devices, such as avionics. These methods provide not only much higher productivity and quality of results, but also offer features such as verification management and requirements tracing through verification—features necessary in a DO-254-compliant flow. Two companies who are leading suppliers of verification solutions, with a focus on the needs of DO-254, include Aldec and Mentor Graphics.

Independent IP Suppliers: Independent suppliers of FPGA IP may be part of a certification network where they offer previously certifiable IP blocks, with sample certification and documentation. They may offer IP test benches as well for DO-254 verification procedures. This brings credibility for using the IP in an operational flight system.

Certification Services: DO-254 certification services typically offer packages that include the PHAC, validation and verification plans and results, HDL source code and the HAS document. H-Cell Engineering is an example of an engineering service company with a strong focus on safety-critical applications in avionics application. H-Cell Engineering performs the whole certification package required for DO-254 for soft IP targeting FPGA technologies.

Programmable Logic and IP Supplier: FPGA vendors can offer IP integration expertise to help with the DO-254 requirements and delivery process for your projects. Altera has participated in the DO-254 Users Group since 2005 in order to discuss best practices, successful implementation results, difficulties, and other issues with aerospace companies. Other FPGA vendors have also joined the Users Group since then.

Because DO-254 is a high-level, process-oriented standard, responsibility for design assurance requires a team approach among designers and suppliers. As such, defense organizations are well advised to seek out team solutions and partnerships with suppliers in order to best meet the needs of their customers. Engineers and engineering managers faced with new DO-254 certification requirements should know they are not alone. Through a team of education, consulting, IP providers, documentation providers and solution providers, DO-254 is a manageable cost risk for defense programs. ▮▮

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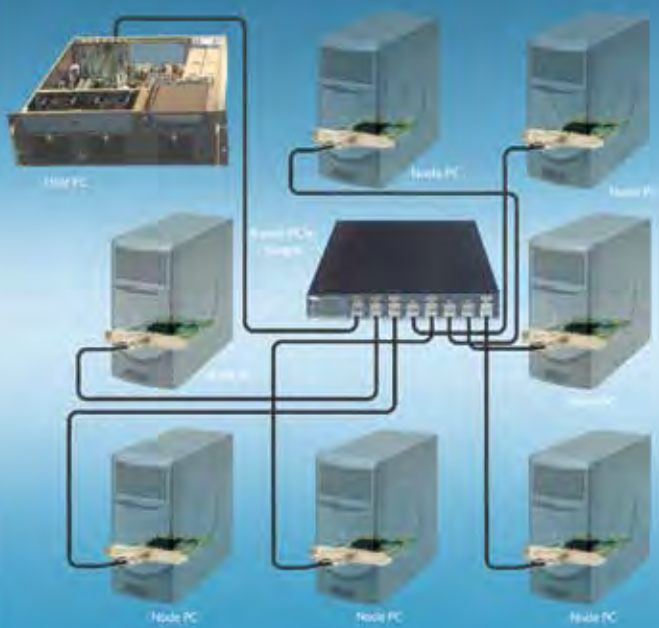

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System Development

USB & PC In Military Test Platforms

USB and the PC Usurp Military Test Platforms

Fading fast are the days when complex military electronics systems required large racks on boards to implement test platforms for them. Now the same test functions can be done on the PC using USB, PCI Express data acquisition and test modules.

Jeff Child,
Editor-in-Chief

Advances in serial fabric interconnects and embedded computing technologies have had a profound effect on the test and instrumentation market. Not too long ago complex military embedded systems, and aircraft in particular, couldn't get through its development phase without bringing to bear heavy-duty test and instrumentation equipment. Today such systems can be pieced together around standard and embedded computer systems. Once that meant large racks of boards—based on VXI and other older form factors. Now the same test functions can be done on the PC using USB, PCI Express data acquisition and test modules. And the PC itself—in desktop, laptop or single board embedded computer form—functions as the platform for running the test software and to serve as user interface. The sidebar "StackableUSB Opens New I/O Door for Military" explores a new spec that leverages USB as a stackable interconnect for PC/104-sized boards.

Recent marriages of standard form factors have further enhanced the performance and modularity available for these applications. CompactPCI and PCI Express have blended into the emerging CompactPCIe. And CompactPCIe has in turn been adopted as the basis for the new version of the PXI instrumentation standard, called PXI Express. This standard allows CompactPCIe boards to be used with instrumentation-specific boards that have additional timing and trigger lines defined.

Exemplifying this trend toward moving to a more integrated test platform, G-Systems took on the task of replacing a proprietary VME-based DSP system owned by Lockheed Martin with a system that acquires, analyzes and stores dynamic pressure data from a next-generation jet fighter engine design. Using industry standard, off-the-shelf technologies including PXI, MXI, UDP and RAID with LabVIEW Real-Time to create a tightly integrated data acquisition and control system that meets stringent technical demands.

The upgrade enabled Lockheed Martin engineers to configure their PXI-based system 10 times as fast as when using their previous VME equipment while doubling their channel count. Also, the Portable Digital Data Acquisition System (PDDAS) reduced test cycle time from 2 sec to 50 ms all for less than it would have cost to upgrade only a portion of the VME-based test system, according to G-Systems. Engineers at Lockheed Martin use scale models of equipment in the testing of the F-35 Joint Strike Fighter (Figure 1). Because their previous VME-based test system proved too difficult to configure and upgrade, engineers at Lockheed Martin commissioned G-Systems to develop the new PDDAS system to control and acquire data from their wind tunnel tests. The PDDAS includes 128 channels of simultaneously sampled dynamic pressure measurements based on two PXI chassis, equipped with a total of 16 NI PXI-4472 Dynamic Signal Acquisition boards.

Figure 1

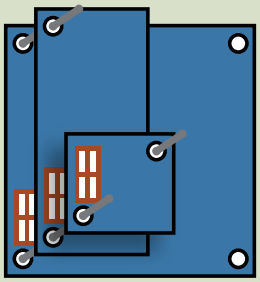
The F-35 Lightning II shown here flying for the first time in December 2006 from Lockheed Martin in Fort Worth. The stealthy F-35 is a supersonic, multi-role, 5th-Generation fighter designed to replace a wide range of existing aircraft.

Test Gear Going Mobile

As the PC shifts into the role of preferred military/aerospace test platform, the result is not only more integrated, less costly systems, but also more mobile systems. When a complex, real-time data acquisition system is small enough to fit in the back of a truck or Humvee, suddenly a whole range of new capabilities opens up.

An example along those lines is Boeing's Quiet Technology Demonstrator 2 (QTD2) project where Boeing flight-tested new technologies intended to reduce the amount of noise aircraft generated. During the first

StackableUSB Opens New I/O Door for Military



One single board computer using StackableUSB can accommodate up to five USB I/O devices stacked on the top side of the board and five on the bottom side, without ever needing the use of a hub and always preserving the star topology of USB.

StackableUSB defines a promising new I/O channel for military and rugged applications requiring small form factor boards. The USB cable from the desktop and laptop world is replaced with stackable board-to-board connectors that support multiple USB ports. This transforms USB into a multi-faceted I/O channel that embedded system designers can use to enhance their embedded applications in a way similar to how PC/104 enabled the ISA bus to be used as an I/O channel.

Microcontrollers, sensors, analog and digital I/O chips, and application-specific ICs are all being released with USB interfaces in increasing numbers. Meanwhile, Intel has just introduced the embedded-friendly Atom processor, which sets the standard for the next generation of small form factor PCs. The ability of the Atom processor to operate on significantly less power will push the marketplace into smaller form factors than the embedded PCs of the past. In addition, the Atom expands internal support of USB to eight internal USB ports from the chip.

These trends are presenting new USB I/O options to embedded system designers looking for an I/O channel that is well supported with silicon, stable over the long run, and reliable in harsh environments. What has been missing in the embedded space is a USB implementation that defines and supports multiple USB ports in a stack that is rugged and cordless so several USB I/O devices can be attached to a single board computer. The StackableUSB standard is filling this need by defining a protocol, specifying a connector, and extending a power specification to maximize USB for harsh, rugged applications similar to those found in military systems.

As StackableUSB emerges as the industry standard for board-to-board communication via USB, a defined protocol ensures boards from one vendor will operate with ones from another vendor. StackableUSB protocol defines up to 10 USB root ports in a single connector. One single board computer can accommodate up to five USB I/O devices stacked on the top side of the board and five on the bottom side, without ever needing the use of a hub and always preserving the star topology of USB (see figure).

The differential connector that implements the StackableUSB architecture was designed for the harsh environments common to test, measurement, industrial, aerospace and military applications. It provides EMI suppression through a shield plate along the sides of the connector and terminating to the PCB itself. It is capable of being hot pluggable when enabled by the single board computer and has been tested and validated for the use in USB 1.0 and USB 2.0 applications.

Power considerations are foremost in any embedded design, as is a preference for power to be from a single source. USB has traditionally powered each device individually and with separate wall-mounted power supplies, which runs counter to the need of embedded systems. StackableUSB eliminates the need for separate power supplies by defining a power specification that provides power from a single source through the USB stack to the individual USB devices. Realizing the 500 mA limit defined for the desktop world was also not sufficient for embedded applications, the power available in the StackableUSB protocol provides almost a full amp (.938 mA) per device. The additional power available for an I/O board dramatically increases the functionality an I/O board can provide to the users.

stage of the QTD (QTD1) project in 2001, Boeing deployed a VXI test system that was limited in both channel count and channel bandwidth. The system required a centralized data architecture that required them to co-locate all the VXI chassis for synchronization, necessitating long cable runs from the microphones to the data acquisition system. That meant about 10 miles of cable per 100 channels of data acquisition. On top of that there were other challenges including time delays when synchronizing instruments across multiple VXI chassis. That meant significant cost per channel, and significant time required for data retrieval.

In contrast, the recent QTD2 phase of the project made use of the flexibility and modularity of PXI to create a scalable system with virtually unlimited channel-count capability. By taking advantage of National Instrument's timing and synchronization cards, the Boeing engineers could distribute the data acquisition hardware into the microphone array, decreasing cabling by nearly 80 percent while maintaining within one degree of phase match between channels. The controller cards were each linked through Gbit Ethernet to one central host computer. That enabled faster post-acquisition data recovery to the host computer and other systems used for data processing and analysis. This unlimited, distributed architecture reduced the cost per channel by more than 50 percent compared to the previous system. ▮▮

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The Case for Mixed-Language Programming

Legacy and functionality issues can be at odds when choosing a programming language for a defense embedded system project. Tool advances now open the mixed-language strategy as an option.

Ole N. Oest, Chief Technical Officer
DDC-I

The DoD lifted its mandate for Ada in 1997. Since then, C and C++ have been the languages of choice for most new defense projects. Still, new Ada designs continue on. Meanwhile, a growing number of military developers has begun to embrace Java, with real-time and safety-critical enhancements making it increasingly attractive for mission-critical applications.

For new projects devoid of legacy code, deciding which programming language to use is a straightforward proposition. The decision can be made entirely on the merits of the language. Most military projects, however, carry with them a substantial amount of legacy code. As a result, deciding which language to use, whether the goal is to streamline maintenance or add new functionality, cannot be done without considering the impact on existing code.

The software used in mission-critical military systems must be reliable, either through system error detection and fail-over mechanisms, or by being inherently fail safe. In order to be fail safe, the software must be deterministic, with no possibility of an unknown or unexpected response. It must also undergo rigorous testing for all possible branches within the software.

The ideal programming language for safety-critical software would allow succinct implementation of the design, avoid error-prone constructs, and ensure a high degree of checking by the compiler. The language should also produce finished code that is 100 percent testable, thereby preventing "dead code" from lingering within the program. Of particular importance for safety-critical software is traceability, which means that actions at the source level can be mapped to the object code and vice versa.

When a language generates branches in the object code that do not correspond to actions at the source level, testing and documentation become more difficult and costly. Newer, more expressive languages like Java tend to offer succinct designs, avoid error-prone constructs, and provide a high degree of checking by the compiler. Older and simpler languages like C tend to fare less well on these three items, but offer superior traceability.

Trade-Offs of Ada

Ada was developed in the late 70s and early 80s under a mandate from the DoD to replace the hundreds of languages then in use in defense applications. In 1987, the DoD mandated the use of Ada for all software projects where new code accounted for more than 30% of the total code.

Ada was designed with safety-critical embedded systems in mind, supporting real-time operation as well as the ability to directly access and manipulate the system's underlying hardware. Ada is a "safe" language, providing features that prevent developers from accidentally creating functions that compromise other functions, and an architecture and tool set that prevents programming errors and/or detects them early in the development process. Ada also has design rules and architectural constructs that simplify and speed code testing. An example project that relied on Ada's advantages is Raytheon's Guidance Electronics Unit (GEU) on the Joint Stand-Off Weapon (JSOW) (Figure 1). The GEU is the operational core of the JSOW. The system's original assembly code was ported to Ada using DDC-I's DACS cross-compiler.

Figure 1

Ada is used in Raytheon's Guidance Electronics Unit (GEU) on the Joint Stand-Off Weapon (JSOW). An F-16C Fighting Falcon shown here releasing an AGM-154 joint stand-off weapon.

Despite its technical advantages, Ada's identity as a military language has limited its widespread adoption. As a result, support for Ada development, in terms of tool availability and numbers of

experienced programmers, has lagged far behind that of contemporary programming languages such as C++ and Java.

Migration to C and C++

As development support for Ada waned, many defense contractors began to migrate their applications to C and C++ in order to simplify maintenance and facilitate future enhancements. C and C++ are popular and have widespread tool support, which helps ensure a steady supply of qualified programmers and powerful development tools. Still, both languages lack many of the capabilities and attributes that were built into Ada for military applications.

In particular, C and C++ lack programming safeguards, which makes them inherently unsafe and complicates military system development. Both languages, for example, require that programs perform heap management, allocating and freeing memory on their own. This can cause errors like memory leaks—a failure to free allocated memory—which eliminate available memory and can eventually lead to software failure.

C and C++ also allow the explicit use of pointers to locations in memory, which can cause a myriad of errors, such as referencing nonexistent objects and altering the wrong memory locations. These errors make it difficult to identify memory leaks and can cause fatal system behavior in the field, yet easily escape detection during program development. To address these shortcomings, larger aerospace and defense developers have added more than 250 design rules to C and C++ development to ensure robust software design. The design tools, of course, must enforce these design rules, or errors will creep in anyway.

Java for Military Applications

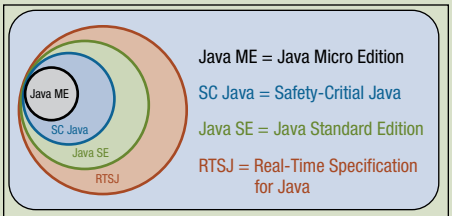
Despite their technical limitations, C and C++ continue to be the languages of choice for new projects as well as migrating existing Ada code. That is beginning to change, however. Java's state-of-the-art development tools and growing legion of experienced programmers have caught the eye of many defense contractors.

Java also offers a number of technical features that facilitate safe programming. The Java structure, for example, enforces object-oriented programming constructs to prevent design flaws. It also takes the risk out of downloading and running application programs of uncertain origin. And its so-called "sandbox" operating environment prevents programs from accidentally interacting, and prevents malicious programs from seizing system control.

For all of these advantages, standard Java also has its shortcomings. Originally designed for non-real-time desktop computers, traditional Java lacks many features that are essential for real-time, safety-critical applications. For example, traditional Java lacks the ability to directly manipulate hardware. Java also lacks determinism.

The Road toward Safety-Critical Java

A relatively new drive within the Java community aims to expand the language's applicability to safety-critical systems. The JSR-302 Expert Group, formed in August of 2006, is now defining a "safety-critical" Java profile (SC Java). This subset of RTSJ enhances reliability by eliminating class libraries and functions (such as garbage collection and dynamic class loading) that can make for unpredictable and unsafe program execution.



Safety-critical Java will be a profile, based on the Real-Time Specification for Java and with a limited API, trimmed to essentials in order to simplify testing.

The JSR-302 Group's approach has been to start with the RTSJ as its basis (see Figure). From there, the JSR-302 Group is taking steps to limit the size of programs and the Java engine by restricting the Safety-Critical Java (SC Java) implementation to the core features that a system must have in order to operate. This reduction will not change the programming language significantly, so SC Java will be easy for today's Java programmers to adopt. Instead, the specification will simply restrict which predefined classes will be available to the safety-critical developer. Some restructuring of Java may also be required in order to avoid the accidental use of forbidden constructs. In addition, programmers will have to follow new programming rules to avoid introducing timing uncertainty.

These changes will eliminate some of the standard features of Java, but give the language greater predictability for program execution. SC Java will also provide the means for avoiding features such as garbage collection, dynamic class loading and just-in-time compilation. In combination, these restrictions will permit replacement of the full Virtual Machine with inline code implementing the actual functions in use, a key to determinism and testability.

The JSR-302 Expert Group's minimum objective is to meet the requirements of the DO-178B standard, Level A, which is used for certifying avionics system software. A draft version of the safety-critical Java specification is nearing completion, with first implementations expected by early next year.

When the definition of SC Java is complete, the JSR-302 Group plans on delivering the specification, a reference implementation and a test suite. The specification will define SC Java as precisely as possible, and is expected to include templates that provide a top-level structure for applications. The reference implementation will provide an example of correctly handling the specification that can serve as a guide for other implementations. The test suite will allow developers to verify that their implementations are in compliance with the specification.

The work of the JSR-302 Group is only a beginning. The industry must provide new analysis tools that will help developers enforce the programming restrictions of SC Java. The industry may also develop SC Java implementations containing additional safety-related features and create application notes showing effective uses of tool sets. These activities are beyond the scope of JSR-302, however, and will fall to individual vendors.

Traceability is also a problem for traditional Java. Java programs run under an interpreter called the Java Virtual Machine, which interprets Java Bytecodes and controls software execution. This can create headaches for safety-critical system designers. Java's breadth of capabilities requires a large interpreter, even though particular Java programs may only require a small subset of the available Java functionality. As a result, Java programs inevitably include unnecessary code that evades testing. Some of Java's automatic features also complicate timing and resource analysis. One of the most significant is Java's automatic "garbage collection," which eliminates memory leaks by automatically freeing unused memory.

Garbage Collection Problem

In some implementations, this operation runs as a background process. As a result, garbage collection is non-deterministic and outside of user control. It can occur at any time. Thus, timing and resource availability may vary from run to run depending on when garbage collection is initiated. Such variability is unacceptable for safety-critical systems.

One way to mitigate the uncertainty of garbage collection is to have the Java compiler intersperse code of its own with the Java source code. This approach can help software developers bound garbage collection in time. But it inserts additional code paths that obscure traceability from the Java source to the final code, thereby making it impractical for safety-critical systems.

Java's real-time and safety-critical limitations have prompted the Java Community to develop specialized Java profiles squarely targeting real-time and safety-critical applications. The Real-Time Specification for Java (RTSJ), for example, makes provisions for bounded application response times, which make Java more deterministic. The RTSJ doesn't address direct manipulation of the underlying hardware. However, these hardware-level tasks can be handled through C.

Real-Time Java provides a variety of safeguards and language features that support mission-critical system software development. These attributes make RTSJ similar to Ada in its ability to address military system requirements while leveraging the wide availability of Java tools and programmers. There is also a new drive within the Java community to expand the language's applicability to safety-critical systems. The Sidebar "The Road toward Safety-Critical Java" details those efforts.

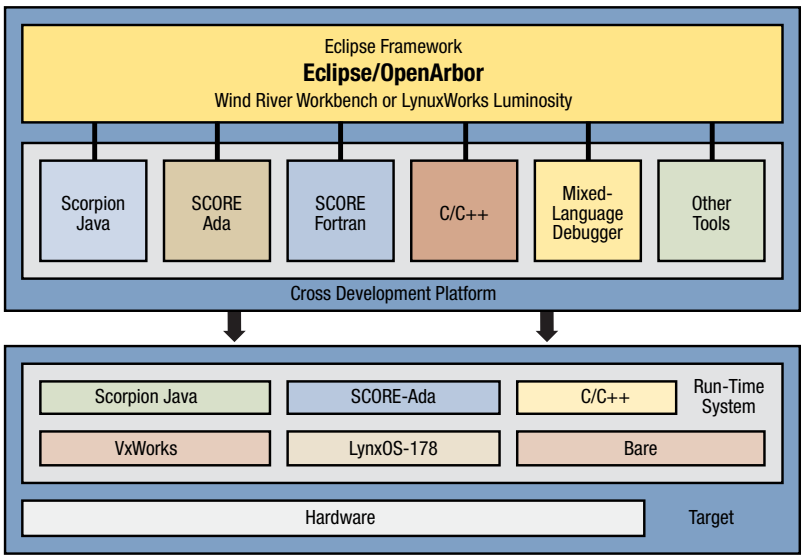


Figure 2

Eclipse-based tools, such as DDC-I's OpenArbor, simplify mixed-language design. Program elements in one language can call program elements in any other language, and developers can compile and debug program elements from multiple languages in the same session.

Changing Languages: A Last Resort

While it may be tempting and desirable to rewrite existing applications in a new language, developers typically prefer to reuse existing code wherever possible, provided that code is still effective. Recompiling existing code in the same language for a new processor, changing development hosts, and switching run-time systems is tough enough. Changing languages can be fraught with risk, invariably introducing unexpected and elusive changes.

Ada, for instance, uses objects, while C does not. C++, meanwhile, uses objects, but in a different manner. Accommodating these differences can easily introduce behavioral changes into the code that alter system operation. Rewriting code also requires that the code be retested, a time-consuming and expensive proposition for mission- and safety-critical systems.

If the original language must be scrapped, system designers can change languages in part through translation tools. Be warned, however, that no tool can do a complete job, and the readability of the converted source program may be questionable. If the designer has no choice, however, he should use a development tool set that supports the old and the new target languages with the ability to mix languages.

Eclipse-based tools, such as DDC-I's OpenArbor, simplify mixed-language design and migration by providing a unified development and debug environment that supports legacy languages such as Ada as well as modern languages like C++ and Java. With OpenArbor (Figure 2), program elements in one language can call program elements in any other language, and developers can compile and debug program elements from multiple languages in the same session. They can use the same tools to debug, upgrade and migrate their applications, regardless of the underlying CPU, run-time system, language or mix of languages. ▮▮

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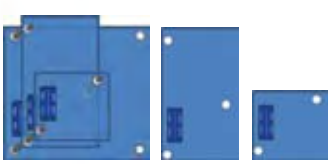

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Technology Focus

Processor Mezzanines

Processor Mezzanine Boards Ascend to New Levels of Performance

Processor-based mezzanine products based on PrPMC, PrXMC and PrAMC continue to ramp up their compute densities and functionality. While PrPMC holds a strong legacy position, newcomers PrXMC and PrAMC are staking claim to the next generation of performance needs.

Jeff Child,
Editor-in-Chief

Because microprocessors and memory—which comprise the computing core of embedded systems—evolve at a much quicker pace than other electronics, the idea of separating computing function from I/O and application-specific function has become a core theme in military applications. In fact, that idea is extremely attractive for applications with long design cycles like the military. Exemplifying that trend are processor-based mezzanine cards. Processor PMC (PrPMC) started that trend by turning the whole rationale of a mezzanine on its head. Where mezzanines were created to provide expansion for standard or custom I/O that attaches to a standard computer base board, the PrPMC idea reversed that thinking. Instead, the Processor PMC becomes the computing core, while the base board that carries it becomes the platform for I/O that's either custom or slow to change or both.

Over the years PrPMCs have won numerous design wins in applications like jet fighter designs, missile guidance systems and UAVs (Figure 1). In all those examples, the PrPMC's size and rugged mechanicals are a key part of the appeal. As mentioned earlier, military designers like how PrPMCs make it easy to upgrade the CPU and main memory in their system over a long life. And there's a more universal factor drawing designers to PrPMCs: system developers are increasingly reluctant to take on computer design efforts with all the associated logistics and support issues involved.

Offering an upgrade path for switch fabric support, the XMC (Switched Mezzanine Card) specification is nearing ANSI approval. The VITA 42 XMC set of standards provides backward compatibility with legacy PMC modules while allowing PCI-bus products to integrate switched fabric architectures. The standards build on the existing PMC standards by adding switched fabric interconnects to the existing PCI bus interface. XMC has a conduction-cooled option that piggybacks off the VITA 20 Conduction-Cooled PMC standard.

Figure 1

PMCs and XMCs are well represented in complex systems such as Raytheon's radar system, known as the Multi-Platform Radar Technology Insertion Program (MP-RTIP). MP-RTIP is used in a number of platforms including the Global Hawk UAV.

Meanwhile, the Advanced Mezzanine Card (AMC) form factor, which also supports processor-based cards—was primarily created as a mezzanine for PICMG's telecom-targeted ATCA form factor. That said, Processor AMCs could gain traction in military application as the slot-card component of the MicroTCA form factor. The MicroTCA system architecture enables AMC cards to be plugged directly into the MicroTCA backplane, so they can be used without a carrier card. The AMC module contains 170 gold-plated pads that are inserted into a female connector mounted onto the MicroTCA backplane. Each AMC module has its own face plate attached to the board, and an ejector handle. MicroTCA's acceptance in the military market is not a sure thing—a lot will depend on ongoing efforts to craft a ruggedized version of MicroTCA to make it suited for harsh environment applications. ▮▮

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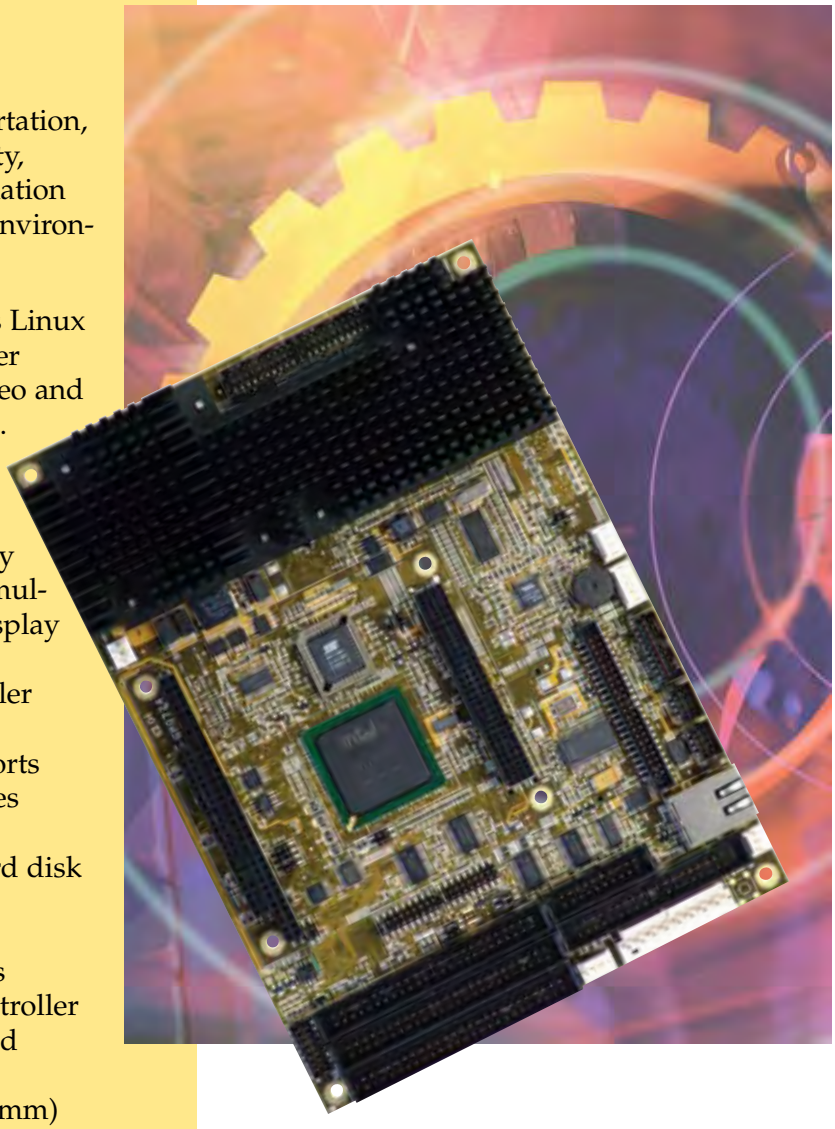

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Technology Focus:

Processor Mezzanines Roundup

PMC Modules Interface I/O to Virtex-5 FPGAs

Performance in mission-critical applications is never purely a measure of computing power. Unless data can be brought off and onto the CPU at a reasonable rate, the added compute muscle is useless. Acromag offers a set of new PMC-VSX modules featuring a DSP-optimized Xilinx Virtex-5 FPGA that is reconfigurable for high-performance I/O processing and user-developed algorithmic computation. For fast data transfer in and out of the FPGA, the PMC-VSX from Acromag provides large banks of DDR2 DRAM and dual-port SRAM for high-speed DMA transfer to the PCI bus. A PCI-X interface ensures plenty of bandwidth to rapidly move data. An assortment of plug-in I/O extension modules offers flexibility to interface various analog and digital I/O signal types.

The PMC base card provides 64 LVDS I/O channels accessible via P4 rear connectors. Inserting optional front-connecting AXM I/O extension modules augments I/O processing capabilities with an efficient interface for 16-bit 105 MHz A/D conversion, CMOS digital I/O, RS-485 differential signals, or extra LVDS I/O lines. Typical uses include video, imaging, radar/sonar, electronic warfare, signal intelligence and communication processing.

This PMC module employs Xilinx's VSX95T Virtex-5 FPGA with 95,000 logic cells and 640 dedicated 18 x 25 DSP48E slices. The DSP48E slice simplifies implementation of high-performance filters and complex math functions. These performance-tuned DSP engines perform up to 352 GMACs at 550 MHz for execution of the most compute-intensive algorithms. Boards start at $6,750 with extended temperature (-40° to 85°C) and conduction-cooled models available.

Acromag
Wixom, MI.
(248) 295-0310.
[www.acromag.com].

AMC Processing Module Features Four TigerSHARC DSPs

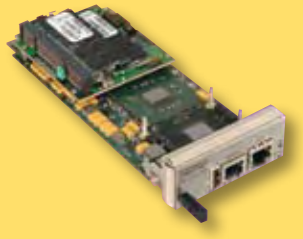
Compute-density remains a major watchword in today's military system designs. Feeding such needs is BittWare's B2-AMC, a Serial RapidIO (SRIO) endpoint solution based on Altera's Serial RapidIO IP Megacore targeting a high-performance Stratix II FPGA. Combining the logic density of Altera's Stratix II FPGAs with the performance of Analog Devices TigerSHARC, and the benefits of AdvancedMC and SRIO, the B2-AMC supports universal baseband processing for any wireless application including Software Defined Radio. The card features a 4x fat pipe running at 3.125 GHz, which can be shared via ATLANTiS amongst the four TigerSHARCs and/or FPGA processing blocks. Eight bi-directional TigerSHARC link ports, running at 4 Gbits/s each, are connected to ATLANTiS providing a tremendous amount of I/O bandwidth and a highly efficient means of dealing with the I/O.

A full-height, single-wide AMC, the B2-AMC, is suitable for use in AdvancedTCA, MicroTCA, or custom systems and is completely hot-swappable. The B2-AMC provides 14.4 GFLOPS and 57.5 GOPS of processing power. The Stratix II FPGA implements BittWare's ATLANTiS framework and the fat pipe interface, seamlessly integrating the DSP processing power with Serial RapidIO, or any other switch fabric (PCI Express, GigE, or XAUI (10 GigE)). Pricing with OEM quantities starts at $4,995.

BittWare
Concord, NH.
(603) 226-0404.
[www.bittware.com].

AMC Processor Provides 2.16 GHz Intel Core 2 CPU

The Processor AMC form factor—particularly combined with MicroTCA—has begun capturing some of the military market's mindshare. Serving those needs, Concurrent Technologies provides its AM 110/10x, an AMC that supports either the 2.16 GHz or 1.5 GHz Intel Core 2 Duo processor to provide high-performance processing, and the Intel 3100 chipset to support up to 8 Gbytes of DDR2 ECC SDRAM. The AM 110/10x is designed for use in a variety of applications including projects within the defense, security and industrial markets. For embedded types of applications there is an option for an onboard application flash disk (up to 8 Gbytes). Accordingly, the AM 110/10x supports a variety of industry standard operating systems.



To enhance overall memory and I/O performance, the AM 110/10x utilizes the Intel 3100 chipset, which combines server-class memory and I/O controller functions into a single component. The Intel 3100 chipset interfaces to up to 8 Gbytes DDR2-400 ECC memory, via two registered SODIMMs, with a peak memory bandwidth of 3.2 Gbytes/s. The AM 110/10x is designed in compliance to AMC.0 (including full hot swap and IPMI capabilities), AMC.1 Type 8 (PCI Express x8), AMC.2 Type E2 (2x Gbit Ethernet) and AMC.3 Type S2 (4x Serial ATA150 ports). The module also features two USB 2.0 ports and an RS-232 port. There is a further Gbit Ethernet port, USB 2.0 port and RS-232 port accessible via the front panel. An optional onboard USB flash disk is available in a range of capacities up to 8 Gbytes.

Concurrent Technologies
Woburn, MA.
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Compatible XMC Modules from Innovative Integration

X5-400M - 400 MSPS 14-bit A/D (x2) • 500 MSPS 16-bit D/A (x2) • 1GB DDR2 DRAM
X5-210M - 210 MSPS 14-bit A/D (x4) • 512MB DDR2 DRAM
X5-GSPS - 1.5 GSPS 8-bit A/Ds (x2) • 512 MB Memory
X3-10M - 25 MSPS 16-bit A/D (simultaneously sampling x8)
X3-25M - 130 MSPS 16-bit A/D (x2) • 50 MSPS 16-bit D/A (x2)
X3-A4D4 - 4 MSPS 16-bit A/D (x4) • 50 MSPS 16-bit D/A (x4)
X3-DIO - 64-bit 66MHz LVDS
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XMC Blends Virtex-5 SXT FPGA and RapidIO

Demanding, high-performance signal and image processing applications, including radar, sonar and signal intelligence, have been hungry to take advantage of the computing power of the Xilinx Virtex-5 FPGA. Along just those lines, Curtiss-Wright offers an XMC module (VITA 42) compute engine based on the Xilinx Virtex-5 FPGA. Called the XMC-442, it is the company's first module to feature the Virtex-5 SXT. The new XMC-442 mezzanine module combines the flexibility of a Xilinx Virtex-5 SXT (SX50T/SX95T) FPGA, the high bandwidth of serial switched fabrics such as PCI Express and Serial RapidIO (SRIO), and rich I/O options.

The XMC-442 works with Curtiss-Wright's CHAMP-FX2 and other Power Architecture-based signal processing engines to enable system designers to integrate tightly coupled FPGA/FPGA or FPGA/PowerPC solutions. The XMC-442 is designed to operate in rugged environments and is available in both air- and conduction-cooled formats. Innovative cooling techniques are employed to handle high-performance FPGA implementations. This XMC daughter card is optimized for deployment on a Curtiss-Wright CHAMP-FX2 FPGA VPX engine, but may also be used on CHAMP-AV6, SVME-184, or VPX6-185 single board computers.

Curtiss-Wright Controls
Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

Dual-Core AMC Breaks Cost/ Performance Barrier

As the U.S. Military builds out the infrastructure for its Net-Centric future, cost-effective, deployable embedded computing is becoming a critical piece of the puzzle. Emerson's PrAMC-7210, an Advanced Mezzanine Card (AMC), provides up to twice the processing capability compared to previous generation modules, for a volume price of under $2,000.

The PrAMC-7210 is designed to provide the best price/performance ratio for a wide range of demanding, low-power embedded applications such as network-centric warfare, digital security surveillance and so on. The PrAMC-7210 is a full-size AMC based on the Intel Core 2 Duo processor core and Intel 3100 server-class chipset. With up to 4 Gbyte double data rate (DDR2) SDRAM with error checking and correcting (ECC) running at 400 MHz and onboard flash disk, the PrAMC-7210 is designed for high performance as well as reliable operation and storage.

One x8 lane PCI Express link supports auto-negotiation to lower lane-widths and port bifurcation. Combined with two Gigabit Ethernet links, these standard interfaces enable developers to interface to a wide variety of high-performance modules as required by their applications. Two SATA links enable high-speed serial communication with hard disks drives for flexible storage configurations. The first PrAMC-7210 modules are priced starting under $2,000 for volume orders.

Emerson Network Power
Tempe, AZ.
(800) 759-1107.
[www.emersonnetworkpower.com].

PMC/XMC Serves Up 1.5 GHz PowerQUICC III

Back when PrPMCs first emerged several years ago most were pretty simple, containing only a processor, main memory and a PCI interface. But today's crop of PrPMCs integrates some of the fastest CPUs available, and a whole lot more. An example is Extreme Engineering Solutions' XPedite5200, a high-performance PMC/XMC communications controller and the first PrPMC to use the 1.5 GHz MPC8548E PowerQUICC III. The processor's integrated 64-bit 133 MHz PCI-X, DDR-2-533 SDRAM, PCI Express/Serial RapidIO and four Gbit Ethernet interfaces make the XPedite5200 an optimal solution for communications processing.

The processor also includes a 512 Mbyte L2 cache and double precision floating point unit as well as two serial controllers and two I2C controllers. Memory provided on the board is up to 2 Gbytes of DDR-2-533 SDRAM and up to 256 Mbytes of NOR flash, up to 2 Gbytes of NAND flash and up to 2 Kbytes of serial EEPROM. The XPedite5200 has two front-panel Gbit Ethernet interfaces and supports two more via the P14 backplane connector. When used as a VITA 42 XMC module, either the x8 PCI Express or x4 Serial RapidIO interfaces can be used, in parallel to or in substitution for the PCI-X interface. Pricing starts at $4,100 in low quantities for a module with 1 Gbyte of DDR-2 SDRAM and 128 Mbytes of NOR flash.

Extreme Engineering Solutions
Middleton, WI.
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[www.xes-inc.com].

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Rugged XMC Offers Choice of Three FPGAs

In demanding signal processing applications, many customers are turning to FPGA technology because of the flexibility and performance it brings. The XMCV5, an XMC mezzanine card from GE Fanuc Intelligent Platforms, is designed for a wide spectrum of digital signal processing (DSP) applications in ground mobile, airborne fixed and rotary wing and naval applications including radar, sonar, signals intelligence (SIGINT) and image processing.

The card lets developers choose from a selection of three Xilinx Virtex-5 FPGAs. The XMCV5 gives customers the flexibility to strike the right balance between hardware-oriented FPGA-based computing and software-based application code running on either PowerPC- or Intel-based platforms as part of a solution based on a range of rugged single board computers, carrier cards, multiprocessors and sensor I/O products. Available in five ruggedization levels—allowing for deployment in the harshest environments—the XMCV5 is the first rugged XMC to harness the power and flexibility of all three Virtex-5 FPGA families with build options for the Virtex-5 FX100T, SX95T and Virtex-5 LX110T. The XMCV5 is available in a range of configurations for rugged air-cooled systems as well as in conduction-cooled form factors.

GE Fanuc Intelligent Platforms
Charlottesville, VA.
(800) 368-2738.
[www.gefanuc.com].

XMC Board Sports Virtex5 FPGA, Four ADCs

FPGAs play a crucial role is applications such as WiMax front ends, radar, electronic warfare and high-speed data recording and playback. Along those lines, Innovative Integration's new X5-210M product is an XMC I/O module featuring four 14-bit 210 Msamples/s A/Ds with a Virtex5 FPGA computing core, DRAM and SRAM memory, and eight lane PCI Express host interface. Xilinx Virtex5 LX110T (SX95T when available) with 512 Mbyte DDR2 DRAM and 4 Mbyte QDR-II memory provide a very high-performance DSP core for demanding applications such as emerging wireless standards. The close integration of the analog I/O, memory and host interface with the FPGA enables real-time signal processing at extremely high rates exceeding 300 GMACs per second.

The X5 XMC modules couple Innovative's Velocia architecture with a high-performance, eight-lane PCI Express interface that provides over 1 Gbyte/s sustained transfer rates to the host. Module functionality can be fully customized using VHDL and MATLAB using the FrameWork Logic toolset, which includes full source code for user FPGA logic device, manuals, documentation and instructions for simulation under ModelSim and recompilation under Xilinx ISE. The X5-210M quantity one pricing is $9,995.

Innovative Integration
Simi Valley, CA.
(805) 578-4261.
[www.innovative-dsp.com].

Complete Core2 Duo SBC Rides AMC

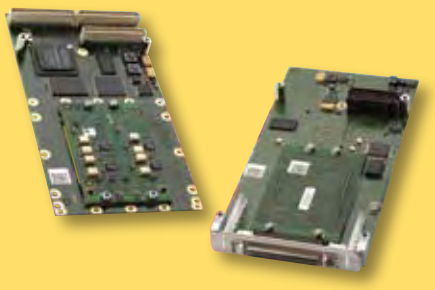
Gone are the days when a computing system required several boards. Now a complete, high-performance SBC functionality is possible in a mezzanine form factor like AdvancedMC (AMC). Along those lines, Kontron offers its AM5010, a highly integrated CPU board implemented as a double-width, mid-size AdvancedMC processor module. The design is based on the Intel Core2 Duo LV 1.5 GHz processor with 4 Mbyte L2 cache providing 667 MHz front side bus (FSB) speed combined with the Intel 3100 server-class chipset. The Intel 3100 chipset is a space-saving, two-in-one solution that incorporates both the Intel Memory Controller (E7320/E7520) and the Intel I/O Hub Controller (6300ESB) in a single package.

The Kontron AM5010 includes up to 4 Gbytes registered Double Data Rate (DDR2) memory with Error Checking and Correcting (ECC) running at 400 MHz, provides up to 8 Gbytes of flash memory via an USB 2.0 NAND flash controller and offers further the capability for an onboard 2.5-inch SATA HDD. Supporting the PICMG sub-specifications AMC.1/.2/.3, the Kontron AM5010 ensures a comprehensive set of interconnecting capabilities. A x4 PCI Express lane (supporting 4 x1 PCI Express as well) according to AMC.1 guarantees high throughput for I/O intensive applications. The dual Gigabit Ethernet supports the AMC.2 specification and utilizes a x4 lane PCI Express interface to ensure maximum packet performance.

Kontron America
Poway, CA.
(888)-294-4558.
[www.kontron.com].

FPGAs Enable Custom PMC and XMC Solutions

Standard mechanical form factors are one thing, but many military applications need their own unique processing configuration. Feeding such needs, MEN Micro now offers its FPGA-based Universal Submodule (USMT) concept on two additional mezzanine cards: the P699 XMC and the P598 conduction-cooled PMC (ccPMC). All products based on MEN Micro's USM concept use one or more IP cores in an FPGA to help designers easily and quickly turn individual I/O requirements into production-ready products reducing design time and costs.



The use of Cyclone FPGAs on the two new cards enables exceptional I/O combinations in a very small space for moderate volumes and at a low cost. The corresponding line drivers are implemented on the individually designed USM submodule that plugs into the main XMC or ccPMC. Because they function independently of other electronic components, the IP cores provide trouble-free, long-term operation over the temperature range of -40° to +85°C (-40° to +185°F). A USM development package includes a main PMC with a USM submodule, test hardware and an FPGA package with a Nios CPU, memory control, connection to the PMC, Avalon/Wishbone bridges and detailed documentation. Pricing for a USM development kit starts at $2,993.

MEN Micro
Ambler, PA.
(215) 542-9575.
[www.men.de].

Single-Wide AMC Boasts Dual-Core PowerPC

Advanced Mezzanine Cards provide the modularity needed in many demanding military communications systems. A single-wide AMC from Mercury Computer Systems, the MPC-102 is a control and signal processing AMC that provides a dual-core e600 Freescale 8641D PowerPC processor at up to 1.3 GHz with up to 2 Gbytes of DDR2 memory, SATA, RapidIO or PCI-E, and Gbit Ethernet connectivity. The dense processing capability of the dual-core 8641D, with a high core frequency, 1 Mbyte of L2 cache per core, and integrated on-chip I/O subsystem with RapidIO, is provided in a flexible AMC form factor supporting 10 Gbit/s raw I/O bandwidth through the RapidIO interface.

The module is AMC.0-compliant and designed to meet AMC.4. The SATA interface supports a HDD in the neighboring AMC bay, making this an ideal host or control node. The architecture and AltiVec vector processing units of the e600 core are compatible with Mercury's industry-leading Scientific Algorithm Library, supporting use of the MPC-102 in dense floating-point processing applications such as radar, sonar and image inspection.

Mercury Computer Systems
Chelmsford, MA.
(978) 256-1300.
[www.mc.com].

Software Radio PMC Offers Beamforming, Power Meter

Real-time software radio, beamforming, signal-intelligence and radar systems all have something in common. They're all hungry for an integrated solution—and that solution does conversion, processing and beamforming all the better. Pentek does exactly that with its Model 7152, a quad 200 MHz, 16-bit A/D digitizer with a 32-channel digital down converter (DDC) configured in a PMC format. The 7152 features 32 power meters that continuously measure the individual average power output of each of the 32 DDC channels. In addition, 32 threshold detectors automatically send an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold.

The built-in power meters and threshold detectors offload these tasks from a downstream processor and present average power measurements for each channel in easy-to-read registers. A second set of new features makes the module ideal for beamforming applications. By adjusting the phase offset and weighting of the individual channels, followed by summation, the antenna can be "steered," rotating the azimuth angle to enhance receptivity in a particular direction. The 7152 PMC module is also available in a variety of additional form factors. The 7152 PMC module is priced at $14,500 for the hardware.

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Tiny SMD Fuse Approved for Space Applications

Reliability and ruggedness take on a whole new meaning for electronics used in space applications. There's no repair truck that can come out and replace failing devices. Schurter has released a new SMD fuse type called the MGA-S that has passed the rigorous ESA/SCC Generic Specification No 4008 for space applications. The MGA-S is based on the design of Schurter's existing MGA. The fuse is hermetically sealed and constructed such that no arcs or gasses can escape with disconnects. Its performance provides consistent pre-arcing times and overcurrent disconnects at rated voltage, regardless of vacuum conditions. Stable derating curves at higher ambient temperatures and durability against mechanical vibration and shock are also requirements of the space industry.

The key differences between a fuse for aerospace and a standard fuse lies in the extensive testing, by means of a "Burn-In" procedure to validate the correct performance of each fuse; the results are recorded. The MGA-S offers a standard 1206 footprint (3.2 mm by 1.55 mm), making it the smallest SMD fuse qualified for use in equipment for space.

Schurter, Santa Rosa, CA. (707) 636-3000. [www.schurter.com].

3U cPCI Card Blends Synchro/Resolver and LVDT/RVDT Sim Functions

The magic of semiconductor integration has fueled the emergence of multi-function boards. Exemplifying that trend, North Atlantic Industries has announced the availability of a 4-channel Digital-to-Synchro/Resolver or Digital-to-LVDT/RVDT Converter on a 3U cPCI card. The 75DS2 3U cPCI card is ideally suited for military and commercial programs, including airborne, shipboard, ground mobile and C3I applications. The DSP-based 75DS2 includes up to four independent, isolated, programmable Synchro/Resolver or LVDT/RVDT simulation channels. Each channel has 16-bit resolution, ±1 arc-minute accuracy, and a short circuit protected output with 1.5, 2.2 or 3.0 VA drive capability. The unit requires +5 VDC and ±12 VDC power supplies, and operates over a frequency range of 47 Hz to 10 KHz.

The 75DS2 provides continuous background Built-In-Test (BIT) on all functions and channels, including reference and signal loss detection. BIT is totally transparent to the user, requires no programming, and doesn't interfere with the normal operation of the card. Each Digital-to-Synchro/Resolver and Digital-to-LVDT/RVDT Converter channel is self-calibrating, without requiring removal of the card. The 75DS2 is available with an operating temperature range of -40° to +85°C or 0° to +70°C. Conduction-cooled versions with wedgelocks are also available. Pricing for 100 pieces of the 75DS2 starts at $2,495 each.

North Atlantic Industries, Bohemia, NY,
(631) 567-1100. [www.naii.com].

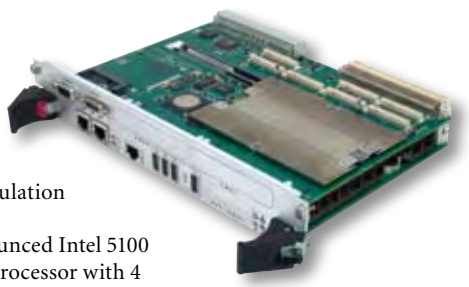
Power Distribution System Aims at Military Vehicles

There's no doubt that military vehicles are being tasked to carry and support an ever growing set of computing and electronics gear. Curtiss-Wright Controls Embedded Computing has announced the availability of the Power Accessory Distribution System (PADS), a ready-to-use, rugged, drop-in power source that delivers 110 VAC as well as 12 VDC and 5 VDC power outlets in 28 VDC power-based military vehicles.

PADS enables soldiers to power a myriad of electronic devices that would otherwise not be supported by their vehicle's traditional 28 VDC power supply, without compromising the vehicle equipment. This compact accessory power system provides power conditioning and power outlets for 110/12/5V common plug items. The rugged, modular PADS system is designed for use in harsh environments. It supports operation over a -30° to +55°C temperature range. Power outlets provided by PADS include dual 12V "cigarette" receptacles, dual 110 VAC utility outlets, dual 5V USB ports and an 18-30V input connector.

Curtiss-Wright Controls Embedded Computing, Leesburg, VA.
(703) 779-7800. [www.cwcembedded.com].

VME SBC Serves Up Intel Quad-Core LV Xeon



For technology refresh and tech update programs, traditional VME is still the major military form factor. And VME vendors continue to roll out new designs for VME. An example is GE Fanuc Intelligent Platforms' new V7812 dual-slot SBC. The V7812 targets military applications that require the quad-core processing performance of the Intel Xeon processor and the advanced capabilities of the ATI Radeon M72 graphics module. Such applications would typically include data encryption, flight simulation control and video compression.

As the first SBC to be designed by the company to take advantage of the capabilities of the newly announced Intel 5100 MCH (Memory Controller Hub) chipset, the V7812 offers either an Intel Dual- or Quad-Core LV Xeon processor with 4 Mbytes of L2 cache to deliver outstanding performance. The V7812 can be optionally ordered as a VXS board, providing an additional Gigabit Ethernet connection routed to P0 in addition to the standard dual Gbit Ethernet connections on the front panel. Support is provided for up to 4 Gbytes of DDR2 ECC SDRAM, six USB 2.0 ports,and four Gbit Ethernet ports (two via optional VXS). A 120 Gbyte 2.5-inch SATA disk or 8 Gbyte SSD SATA drive can optionally be configured on the board.

GE Fanuc Intelligent Platforms, Charlottesville, VA. (800) 368-2738. [www.gefanucembedded.com].

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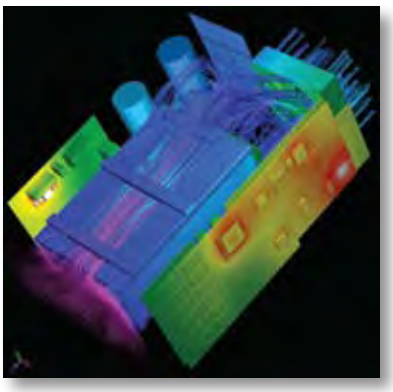


Tool Does Thermal and Flow Analysis IC Package Modeling

It's impossible to avoid the trend toward processors and other key components ramping up in wattage. More power means more challenges dissipating heat. Fortunately tools are available that enable military system designers to analyze and model the thermal performance of their systems. Daat Research has added tools for modeling IC packages into its Coolit v.8 CFD thermal analysis software. The tools build detailed parametric chip models that can be converted to compact models, and the user can switch between detailed and compact models as desired.

Included is a library of hundreds of popular Ball Grid Arrays (BGA), Dual Inline Packages (DIP) and Quad flat Packages (QFP). The user can copy and modify the models, or add new models to the library. Coolit v.8 also delivers many improvements in algorithms for computation and presentation of results. These and many other enhancements make Coolit even more user-friendly and powerful to use. Coolit v.8 is now shipping.

Daat Research, Hanover, NH. (603) 643-2999. [www.daat.com].

VXS Star Backplane Has Eight Slots

The VXS architecture marries the best of both worlds of VME legacy support and switched fabric performance. The military is already using it in a variety of applications where that "here today" level of performance is required. Elma Bustronic Corporation has developed a new size for its line of VXS Backplanes. The 8-slot VXS Backplane features a Star routing topology and fits in most 4U high horizontal mount enclosures.

The 8-slot Star VXS Backplane complies with the VITA 41.0 specifications. It features one hub slot and seven payload slots in a 14-layer controlled-impedance stripline design. Backplane simulation confirms strong signal performance. The 6U high backplane has power studs in 3.3V, 5V, 12V and GND along the top and bottom of the backplane to allow for flexible power options. Bustronic also offers VXS Star backplanes in 5 slots and an 8-slot with one hub, 5 payload and 2 legacy VME64x slots. Dual Star topologies include versions in 8, 12, 18, 20 and 21 slots. Pricing for the 8-slot VXS Star backplane is under $1,500 depending on volume and configuration requirements.

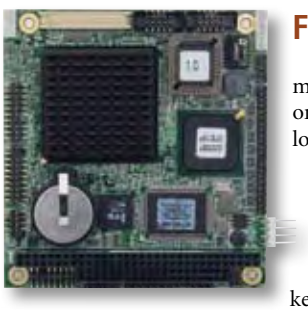
Elma Electronic, Fremont, CA. (510) 656-3400. [www.elma.com].

Chipset Is Optimized for High-Frequency DC/DC Apps

In this age of distributed power and mixed voltage levels, power system design is getting ever more complex for military system designers. International Rectifier eases the way by introducing a 25V synchronous buck converter DirectFET MOSFET chipset for point-of-load (POL) converter designs. The new 25V chipset combines IR's latest-generation HEXFET MOSFET silicon and benchmark DirectFET packaging technology to deliver a high-density, single control and single synchronous MOSFET solution in the footprint of an SO-8, and with slim 0.7 mm profile.

The IRF6710S2 is ideally suited as a control MOSFET due to the device's very low gate resistance of 0.3 ohms and very low Miller charge (Qgd) of 3.0 nC, which significantly reduces switching losses. The IRF6795M and IRF6797M feature extremely low RDS(on) to significantly reduce conduction losses while the integrated Schottky reduces diode conduction losses and reverse recovery losses, making these devices well suited for high-current synchronous MOSFET circuits. Pricing for the IRF6710S2TR1PbF begins at $0.66 in 10,000-unit quantities. Pricing for the IRF6795MTR1PbF and IRF6797MTR1PbF begins at $1.35 and $1.65 respectively each in 10,000-unit quantities.

International Rectifier, El Segundo, CA. (310) 726-8512. [www.irf.com].



Fanless PC/104 Card Sports 500 MHz Geode LX800

The PC/104 form factor with its compact size and inherent ruggedness continues to be a favorite for space-constrained military applications. Diamond Systems announced its latest PC/104 form factor single board computer, Rhodeus, based on the AMD LX800 processor. Rhodeus offers mid-range computing power in a compact, low power consumption and low cost PC/104 single board computer.

Rhodeus is based on the AMD Geode LX800 processor operating fanless at 500 MHz. It includes 64 Kbyte L1 cache and 128 Kbyte L2 cache. The board supports up to 1 Gbyte of DDR SDRAM using a SO-DIMM socket. It provides both IDE and CompactFlash mass storage options. Video consists of an integrated VGA controller with 2D acceleration and support for high-resolution CRT and LCD displays. A full set of I/O is provided to support application requirements, including Ethernet, UDMA-33 IDE, two USB 2.0 ports, one RS-232 and one RS-232/422/485 serial port, floppy, legacy keyboard and mouse, and programmable watchdog timer. Power consumption is 5W typical, and operating temperature is 0° to 60°C. The board includes the PC/104 ISA bus for additional I/O expansion. The Rhodeus single board computer is available immediately. Prices start under $350 in small quantities for models with 256 Mbytes of DDR SDRAM.

Diamond Systems, Mountain View, CA. (650) 810-2500. [www.diamondsystems.com].

Signal Generator Does Delay and Width Control on Eight Channels

When engineering budgets get tight, using test instrumentation that supports a variety of uses makes a lot of sense. Berkeley Nucleonics has made an upgrade in the timing circuitry on the cost-saving Model 505 Pulse / Digital Delay Generator. This Model 505 is now shipping standard from the factory with 10nS delay and width resolution. This model represents an excellent value for users who need multiple channels of timing to gate, delay, synchronize or pulse various components to a research experiment. The 10nS edge resolution is available on all 16 edges (8 Channel Model). Delay and Width control on all eight channels with 10nS resolution gives users the ability to address a handful of devices using a single Pulse / Delay Generator.

The Model 505 gives users up to eight fully defined pulse channels with 10nS resolutions for both delay and width. Gate widths are also achievable as narrow as 10nS. The product ships from stock, includes RS-232 and GPIB, and is priced at $1,990 for two Channels of Delay + Width, $2,496 for four Channels of Delay + Width, and $4,098 for eight Channels of Delay + Width.

Berkeley Nucleonics, San Rafael, CA. (800) 234-7858. [www.BerkeleyNucleonics.com].

Ethernet Device Server Talks to RS-232/422/485 Ports

The military has warmed to Ethernet in a big way. It's a useful means to talk to a wide array of serial I/O. The Industrial Automation Group of Advantech introduces the EKI-1524 Serial Device Server, which is the latest addition to the EKI-1500 family, allowing up to four RS-232/422/485 serial devices to be remotely monitored, managed and controlled over Ethernet and Internet Protocol (IP) networks. Equipped with dual 10/100Base-TX Ethernet ports and dual Media Access Controllers (MACs), this innovative device ensures data transmission even in the event of a network link failure.

The EKI-1524 offers a number of conventional operating modes that allow connections to be initiated by either attached serial devices or remote Ethernet hosts using both UDP/IP and TCP/IP protocols. The EKI-1524 Serial Device Server is packaged in a compact and thin DIN-rail mount chassis. They are ruggedized for demanding industrial applications with 4,000 VDC Ethernet ESD protection, dual 12 to 48 VDC power inputs with power line surge (EFT) protection of 3,000 VDC, and feature an operating temperature range of 0° to 60°C to ensure system uptime.

Advantech, Irvine, CA. (949) 789-7178. [www.advantech.com].

19-Inch Rack Cases Boast Rugged Frames

There's been a slow shift among military customers whereby they're asking for ever more complete and integrated systems. This often means providing the system completely with the enclosure and racks. A new family of 19-inch rack cases from Hammond Manufacturing is available in 1, 2 and 3U heights and depths of 8 inches (203 mm), 13 inches (330 mm) and 18 inches (457 mm). The cases are suitable for housing a wide range of equipment, either mounted in a 19-inch rack or, if required, the units can be used as a desktop enclosure.

The all-aluminum construction consists of a heavy-duty extruded frame, removable vented or plain top and bottom covers and optional 19-inch rack mounting angles and self-adhesive rubber feet. The front and rear panels are removable and interchangeable; they are of flat construction to make machining and screening a simple process. Front panel handles that mount to the rack mounting angles are optionally available to assist with insertion and removal from a rack; to provide greater support for heavy loads, rear-mounting brackets can also be specified. The RM family is finished in durable black powder coat paint as standard.

Hammond Manufacturing, Cheektowaga, NY.
(716) 630-7030. [www.hammondmfg.com].

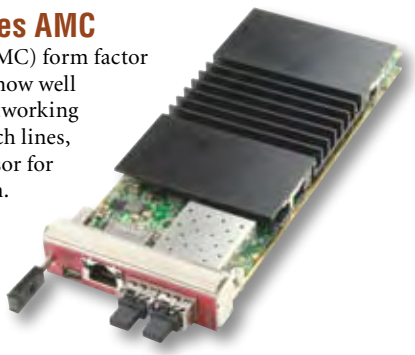
Board Family Tests PCIe Slots Via IEEE Std. 1149.6

Military test systems no long require the complexity of a mass of racks and boards. Now quite a bit of test and debug functionality can be done on the desktop using PCI Express. Along just those lines, Goepel Electronic recently introduced the CION Module /PCIe-x(1/4) family as additional interface cards within the popular CION Module product range. The new low-cost modules are plugged directly into a x1 or x4 PCI Express slot and controlled by means of a TAP (Test Access Port). Because of the onboard IEEE 1149.1 and IEEE1149.6 test channels, all high-speed signal pins, low-speed signal pins and voltage supply pin of PCI Express-compliant connectors are structurally testable.

The CION Module /PCIe-x1 and the CION Module /PCIe-x4 are plugged directly into the connector to be tested. They are able to completely test PCI Express Standard V2.0-compliant slots via dot1/dot6 for correct pin contacting. Because the modules provide transparent TAP, several CION modules of the same or different type can be cascaded due to the daisy chain principle. Altogether, the CION Module product family already has ten different models for the flexible test of numerous analog and digital interfaces.

Goepel Electronic, Jena, Germany. +49-3641-6896-739. [www.goepel.com].

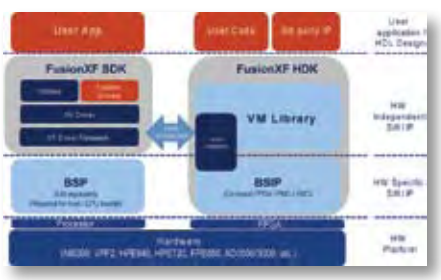
Dual-Port 10 GbE Packet Processor Rides AMC



The acceptance of the Advanced Mezzanine Card (AMC) form factor among military system developers will depend a lot on how well MicroTCA gains mindshare in this market. Comms/networking functions are where AMCs particularly shine. Along such lines, VadaTech has introduced the AMC220, a packet processor for Dual10-Gbit Ethernet based on the AMC.1 specification. This two-port module is offered in a mid-height form factor with the option to order the full-height design. Pre-configured as a TCP Offload Engine, this AMC provides socket layer services to a Cavium OCTEON CN56xx/CN57xx Multicore processor, and can be loaded either by a four-lane PCIe interface or optional flash memory. This host processor enables the AMC220 to process Ethernet packets at line rate while reducing the overhead associated with new standards for packet processing on embedded CPUs.

The AMC220 has options for six to twelve processor cores and is available from 600 MHz to 1 GHz speed grades. Compliance with the newest IPMI version 2.0 allows for manageability that is independent of the operating system, which is supported by Linux, Windows, Solaris and VxWorks. The two RJ-45 micro USB connectors for both USB and RS-232 are located on the front panel of the AMC alongside two SFP+ connectors. The basic configuration pricing of the AMC220 starts around $2,000.

Vadatech, Henderson, NV. (702) 896-3337. [www.vadatech.com].



FPGA Development Kit Eases DSP System Design

FPGA computing has a had a tremendous impact on a variety of military applications like radar, sonar, SIGINT and anything that calls for a dense amount of signal processing. Easing the process of FPGA system development, VMETRO has rolled out its FusionXF FPGA development kit. FusionXF is targeted at reducing the design time and optimizing the performance of complex FPGA and PowerPC processing systems.

FusionXF includes FPGA HDL functions, software APIs, drivers, utilities, example designs and documentation to simplify the task of integrating FPGAs into an embedded real-time DSP system design. It provides the building blocks to build a fully functional FPGA design that a customer can easily integrate their FPGA algorithms and logic into. FusionXF enables the control and utilization of FPGA resources from PowerPC processors and efficient data streaming within a single FPGA and between processors and FPGAs in a system. With the core functionality and glue logic to create a fully functional FPGA design provided by FusionXF, valuable project time can be spent implementing application-specific functionality, e.g., optimizing computational algorithms. FusionXF is currently supported on VMETRO's VPF2 (VXS) and HPE640 (VPX) hybrid PowerPC and FPGA boards, FPE650 quad-FPGA VPX board, and AD1500 and AD3000 A/D XMC/PMC modules.

VMETRO, Houston, TX. (281) 584-0728. [www.vmetro.com].

Command Center Consoles Ready for Rugged Duties

Today's military is highly reliant on computing and communications gear. That means the command center gear most follow suit. With just that in mind, the Mobile infrastructure solutions from Optima EPS include full command centers down to cabinets geared for mobile applications. A new line of consoles, desk systems and enclosures for the mobile command and communications markets addresses applications in battlefield command, law enforcement/HSS, emergency services, mobile labs, and more. The command centers are based on the latest human engineering concepts and ergonomic designs to ensure optimum "usability."

Based on standard modules, the range can easily be modified to suit most applications and ensures optimum access to critical information in command and control environment. Optima's full range of cabinet enclosures can be ruggedized for mobile applications. This provides a wide range of highly ruggedized, Mil-Spec, seismic, datacom, or cost-effective standard platforms to choose from. Optima's console design permits peripheral equipment to be installed using standard EIA rack mounting rails that can support over 300 lbs of equipment. Highly ruggedized versions are optional. Pricing for basic configurations of Optima's command centers starts at under $3,000 and varies widely depending on size and design needs.

Optima EPS, Tucker, GA.
(770) 496-4000. [www.optimaeps.com].

15W DC/DC Converter Series Features Wide Input Range

Military power system designers like to think in blocks. That's why modular DC/DC converters play such a major role in military distributed power architectures. Martek Power announced the release of the 1500UFR series of highly efficient DC/DC power converters. The 1500UFR series is a family of low-noise single and dual DC/DC converters. Packing up to 15W of power into a low profile 2 x 1 x 0.4-inch package with efficiency up to 86%, the series offers ultra wide input ranges of 9-36 VDC, 18-75 VDC and 4:1 input range, and is available in output voltages of 3.3, 5, 5.1, 12, ±12 or ±15 VDC.

The modules are specially designed to address the application needs for data communication equipment, mobile battery-driven equipment, distributed power systems, communications equipment, mixed analog/digital subsystems and robotic systems. The 1500UFR are priced at $20.20 per unit for volume orders. The 1500UFR modules are available in a RoHS-compliant version.

Martek Power, Torrance, CA. (310) 202-8820. [www.martekpower.com].

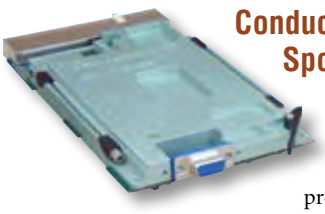
Fanless, Rugged Display Computer Aims at Harsh Apps

The net-centric operations trend in the military is boosting demand for display-based computer terminals to fill out the various endpoints of the network. The DC1 from MEN Micro combines the new Intel Atom processor with aluminum construction to provide a low-power, highly reliable computer that withstands the harsh environments found within many mobile, mission-critical and harsh applications. This is a fanless display computer that is both rugged and maintenance-free.

Because the control electronics are located directly behind the display, the DC1 employs conductive cooling between the electronics and the display, eliminating the need for a cooling fan. The DC1 enables variations in display resolution and size, processor type, I/O configuration and power supply, so users can tailor the system to specific applications. The DC1 comes standard with a 15-inch display with optional display sizes from 12 to 19 inches available as well as with a wide range of power supplies. The design is also tamper-proof to deter vandalism. All components of the IP54-protected DC1 are soldered and only M12 or D-Sub I/O connectors are used. The electronics are prepared for coating to withstand humidity. Pricing for the DC1 is $3,132 for a single unit.

MEN Micro, Ambler, PA., (215) 542-9575. [www.menmicro.com].

Conduction-Cooled cPCI SBCs Sport 1.5 GHz Core2 Duo LV



Multicore/dual-core systems have moved from exotic to mainstream in the military embedded systems. An early adopter of Intel dual-core processors, Kontron's latest is the ITC-320 3U CompactPCI CPU boards featuring three types of single and dual-core Intel processors in four different designs, including a rugged conduction-cooled version for reliable operation in even the harshest environments. The first version comes equipped with the latest dual-core 1.5 GHz Intel Core2 Duo LV processor.

Using the 1.2 GHz Intel Core Duo processor on the Kontron ITC-320 provides the performance-per-watt ratio for applications that need to balance computing performance with low power consumption. The Kontron ITC-320 series also supports the 1.0 GHz Intel Celeron M processor, which is an appropriate choice when power dissipation is a critical issue. The Kontron ITC-320 series features all the I/Os that are available on the latest laptop PCs such as the UXGA graphics controller with PCI Express, two Gbit Ethernet network interfaces configurable by software either on the front RJ-45 connectors or on the rear J2 connector, quad SATA 150 ports and quad USB 2.0 ports. The rugged conduction-cooled version of the Kontron ITC-320 series of CompactPCI CPU boards enlarges the application range of the product for harsh environments.

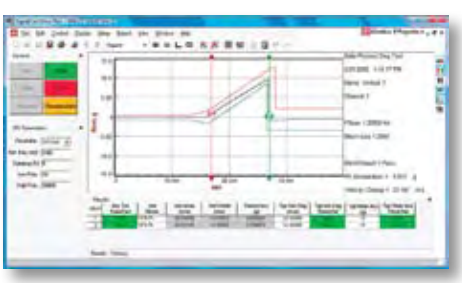
Kontron, Poway, CA. (858) 677-0898. [www.kontron.com].

600W MicroTCA Power Modules Support AC or DC

The new MTC600 series power modules from Emerson Network Power are compact self-contained power solutions for MicroTCA systems. They are compliant with the PICMG MicroTCA.0 Revision 1.0 specification and are available in AC-input and DC-input versions. The MTC600 series MicroTCA power modules are high power density, single-width units; the AC-input MTC600-AC version is 12 HP high and the DC-input MTC600-48 version is 9 HP high. The MTC600-AC has an input range of 90 to 264V, making it suitable for use with single-phase supplies virtually anywhere in the world, while the MTC600-48 has an input range of -39.5V to -72V, which accommodates both -48V and -60V battery plants.

Both versions of the MTC600 power module provide 16 output channels, each capable of delivering 12V at 7.6A of payload power and 3.3V at 150 mA of management power. This is sufficient for a complete MicroTCA system comprising up to 12 AdvancedMCs (AMCs), two MicroTCA Carrier Hubs (MCHs) and two Cooling Units (CUs). Pricing starts at $865 for the MTC600-AC and $825 for the MTC600-48 (100s).

Emerson, St. Louis, MO. (314) 553-2000. [www.emerson.com].



Drop Test Software Does Shock Assessment

Knowing just how rugged a system is requires numerous tests, drop testing among them. Along such lines, Data Physics offers a package for applications such as product fragility assessment, prototype testing and cushion evaluation. This latest addition to the SignalCalc analyzer platform works with drop and/or shock test machines. The new Drop Test application software provides users with the ability to capture and display drop waveforms, perform 'fairing' and pass/fail testing relative to tolerances specified in accordance with industry, military or user-defined standards. The package offers unlimited display layouts, automated reporting and optional shock response spectrum (SRS) measurements.

The base package contains the most essential Drop Test features including transient waveform capture, standards-based or user-defined tolerance limit checks, waveform fairing and velocity change calculations, manual movement of tolerance lines around a captured waveform and the calculations of resultant shock magnitudes for triaxial sensors. The advanced Drop Test option adds SRS analysis capabilities to the base package. The new application comes equipped with internal signal generators that allow the user to simulate actual drop tests with classical waveforms such as half sine, saw tooth and trapezoid.

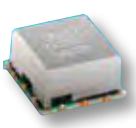
Data Physics, San Jose, CA. (408) 437-0100. [www.dataphysics.com].

3.5-Inch SBC with Geode LX800 CPU Draws 10W

Size, weight and power keep moving further to the top of many of today's military design requirements. With just that in mind, the new MSB800UL from Digital-Logic is a 3.5-inch single board computer (SBC) based on a 500 MHz AMD Geode LX800 processor that is said to provide performance equivalent to that of an 800 MHz chip. To optimize cooling, the processor is located on the underside of the board, enabling a direct connection to the housing. So passive cooling does not have to be set up.

The board provides standard PC interfaces and an additional 10/100BASE T Ethernet LAN. In contrast to the PC/104-Plus cards, all interfaces are connected to standard plugs; this means low-cost, cable-free housing integration. The SBC uses the Geode CS5536 chip set. The main memory of the MSB800 can be equipped with SODIMMs in the range of 128 Mbytes to 1 Gbyte. The video controller that is integrated in the Geode processor supports VGA displays with up to 1600 x 1200 pixels. The SBC has dimensions of 146 mm x 102 mm x 20 mm (L x W x H) and weighs only 0.2 kg. Designed for low power consumption—typically 10 watts—the MSB800UL operates within the temperature range of 0° to +60°C. A MTBF (Mean Time Between Failure) value of more than 200,000 hours confirms the high level of reliability and the long life cycle of the single board computer.

Digital-Logic, Luterbach, Switzerland,
+41 (0)32/ 681 58 40. [www.digitallogic.ch].



Coaxial Resonator Oscillator Boasts Compact Package

Oscillators are critical components for military applications like digital radio equipment and satellite communications systems. Serving such needs, the CVCO38CC-3660-3700 from Crystek operates is a coaxial resonator oscillator packaged in the super-compact 0.380-in. x 0.380-in. x 0.220-in. SMD package, achieving 42% space savings over the standard 0.5-in x 0.5-in package. The CVCO38CC-3660-3700 from Crystek operates from 3660 MHz to 3700 MHz with a tuning voltage range of 0.3 VDC to 4.7 VDC. The CVCO38CC family is available in models that operate from 2.2 GHz to 4.4 GHz in bands. This coaxial VCO features a typical phase noise of -108.69 dBc/Hz at 10 KHz offset and has excellent linearity.

It exhibits an output power of +4.0 dBm typ. into a 50 ohm load with a supply of +5.0 VDC and a typical current consumption of 30 mA. Pushing and Pulling are both minimized to 1.0 MHz/V and 2.5 MHz, respectively. Second harmonic suppression is -15 dBc typical. Pricing for the CVCO38CC-3660-3700 will start at $15 ea. in volume.

Crystek Ft. Myers, FL. (239) 561-3311. [www.crystek.com].

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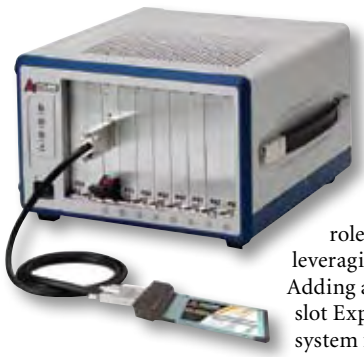
Solid State Disk PCI RAID Adapter Has High MTBF

As program and data needs ramp up in military applications, so too does the demand for rugged high-performance RAID storage. The LT-PCI-CF from Lauron Technologies is a high-performance PCI 64-bit, 66 MHz, 4-channel SSD RAID adapter that supports data rates of up to 533 Mbytes/s. This is a single slot adapter available in 2 Gbyte to 128 Gbyte capacities and is populated with a fast, reliable Compact Flash module. Since the adapter houses all SSD memory, the LT-PCI-CF provides a single card solution for non-rotating media requirements.

The unit has an MTBF greater than 1,000,000 hours provided by built-in EDC/ECC and Wear Leveling algorithms. The endurance with Erase/Write Cycles is greater than 1,000,000. The benefit of the Built-in Flash SSD controller/bridge is that it supports Ultra DMA modes, which yield data transfers at speeds of up to 133 Mbyte/s per channel. The LT-PCI-CF supports RAID 0, RAID 1, RAID 0+1, RAID 5 or JBOD. Stripping modes transfer data to all four channels simultaneously while mirror modes transfer data on both channels. The LT-PCI-CF is shipped with Windows and Linux Device drivers along with RAID management utilities.

Lauron Technologies, Naples, FL.
(239) 431-6237. [www.laurontech.com].



Extension Kit Expands Links to PXI from a Laptop

The days when it took large racks of slot-card boards to implement a military test system are long gone. Now the same role can be filled by PC-based cards, leveraging the speeds of PCI Express. Adding a link to PXI as well, is a multi-slot ExpressCard-to-PXI extension system from ADLINK. The EC-8560/PXI-8565 extends more PXI slots from an ExpressCard-based laptop computer via a shielded cable connection up to seven meters (23 feet) in length. PXI devices installed in the extension PXI chassis behave and work as if they are directly installed in the host system and do not require any additional driver or software installation.

The EC-8560/PXI-8565 implements PCI Express-based control of PXI modules and consists of the EC-8560 ExpressCard extension card installed in a laptop computer, a shielded cable, and the PXI-8565 PXI remote extension card. The EC-8560 is in the ExpressCard/34 form factor, uses one x1 lane, and communicates with the extension PXI chassis via a shielded twisted copper cable. The PXI-8560 remote extension card then converts the PCI Express signal into a 32-bit/66 MHz PCI interface for additional PXI slots.

ADLINK, Irvine, CA. (949) 423-2354. [www.adlinktech.com].

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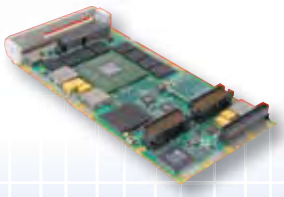

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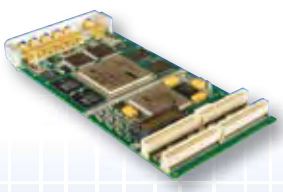

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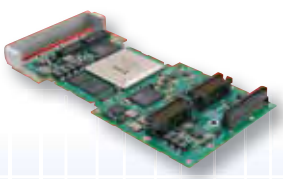

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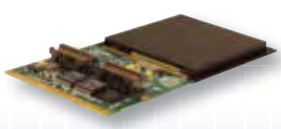

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COTS View

Military UPS Trends

Many Factors Drive Uninterruptible Power Supply Choice

Numerous factors come into play when choosing the best UPS for military applications. These include everything from distortion level to battery capacity to DC offset parameters.

Michael A. Stout, Vice President of Engineering
Falcon Electric

The process of finding, selecting and qualifying commercial off-the-shelf Uninterruptible Power Supplies (UPSs) for military applications can be an exercise in frustration. Manufacturers' specifications and datasheets are written primarily for commercial business markets. They often do not reflect the wider spectrum of information needed to properly determine their applicability for use in a specific military application.

There are three industry standard UPS design topologies: off-line, line-interactive and on-line. For most military applications, the off-line and line-interactive designs are low-cost designs and are not acceptable. They were designed to provide basic battery backup. These types of units simply pass the utility power through the UPS until utility power is lost at which time they turn on and switch to battery-powered inverter operation.

In contrast, the advantages of a good on-line UPS are many. They provide a continuous duty inverter with a low distortion true sinewave output (3% THD typical). Their wide input voltage range marries well with a tight output voltage regulation—around ±2-3% typical. They also provide wide input frequency range while providing tight output frequency regulation. As the inverter is continuously providing the UPS output, there is no disruption of output power when the utility voltage is lost or returns. Meanwhile, battery mode operation time can be lengthened by adding more battery capacity. In some cases, the UPS may also be used as a frequency converter providing a 50, 60 or 400 Hz output independent from a 50, 60 or 400 Hz input. On-line UPSs also eliminate the widest range of utility and generator source power problems. Figure 1 shows an on-line UPS and the sinewave input and output waveforms.

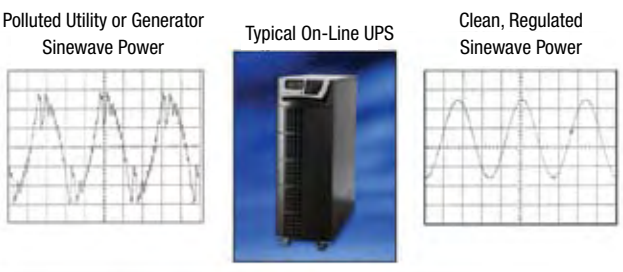
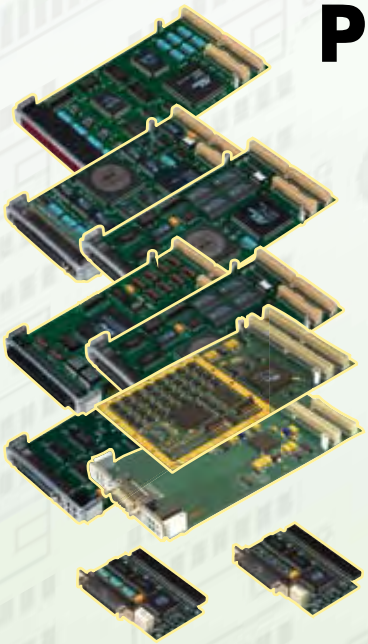


Figure 1
An on-line UPS provides a continuous duty inverter with a low distortion true sinewave output. Their wide input voltage range marries well with a tight output voltage regulation—around ±2-3% typical. They also provide wide input frequency range while providing tight output frequency regulation. Shown here is an on-line UPS and the sinewave input and output waveforms.

PCI-to-PMC

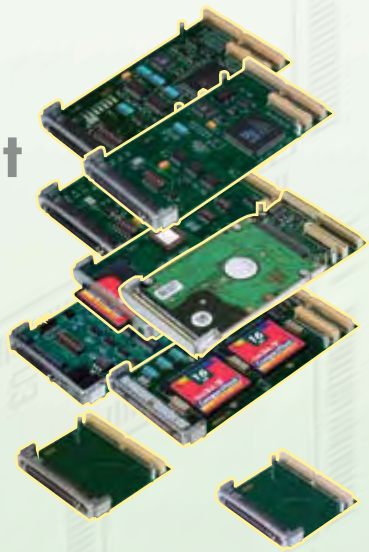


Serial

Ultra320

FPGA

Quad Ethernet



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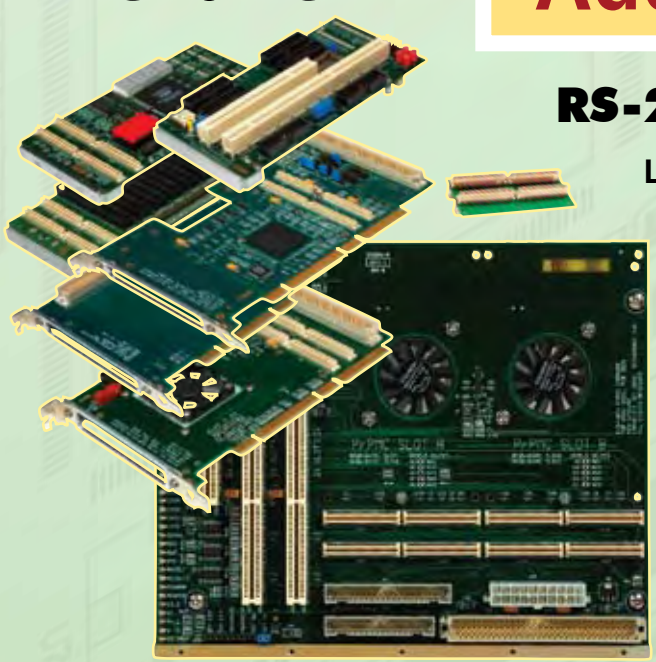

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Construction Concerns

Most off-the-shelf UPS models available are not designed to meet the rigors of full Mil-Spec requirements. With modifications, some models can be made fairly rugged. As part of the engineer's initial investigations, care should be taken to verify the basics. The UPS market is very competitive and as such, some products available are not constructed using double-sided FR4 type laminated circuit boards. The manufacturer has cut costs by using inferior "chopper glass" board material. Even worse from a shock and vibration standpoint, they have used single-sided circuit boards without being plated through.

Circuit board, transformer, battery and heatsink mounting practices could be other areas of concern. Most good quality off-the-shelf on-line UPS products have been designed to withstand the normal shake and vibration sustained during shipment, which can be substantial. Continued trips across the desert in a Humvee (Figure 2) is another matter. The unit may require substantial modifications or even a mechanical redesign to meet more stringent military specifications. If the required quantities are large enough, the manufacturer may be willing to make the changes providing a timely and cost-effective UPS solution to the engineer's requirement. If not, there are other UPS companies offering build-to-order pre-ruggedized off-the-shelf products.

Figure 2

Many good quality off-the-shelf on-line UPS products have been designed to withstand the normal shake and vibration sustained during shipment. But continued trips across the desert in this Humvee is another matter. The unit may require substantial modifications or even a mechanical redesign to meet more stringent military specifications.

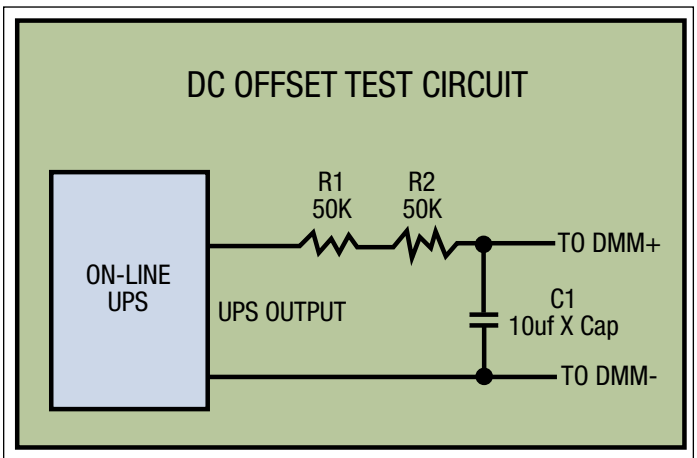

Figure 3

Shown here is a DC offset measurement circuit for an on-line UPS. DC offset is a very important consideration, especially if the UPS is to have a transformer connected to its output. A good UPS will have a DC offset of less than 50mv.

Environmental Concerns

Most domestic off-the-shelf UPS products available are tested to meet or exceed the UL1778 safety standard. As such, they are designed and intended for use in a protected environment. This means that they are not weatherproof, they do not come equipped with protective air filters, and importantly, they have not been tested by UL for operation in a wide temperature range—only within 32° to 104°F (0° to 40°C) with a non-condensing humidity of 10% to 95%. Should the military application be inside a temperature-controlled shelter, this may not be a problem. The fact is that some well designed on-line UPS electronics, if provided enough cooling, would operate over a temperature range of 14° to 122°F or (-10° to 50°C).

For the standard Valve Regulated Lead Acid (VRLA) batteries typically used in off-the-shelf UPS units, it is another issue. Battery manufacturers state that if these batteries are operated or stored in temperatures above 90°F, they will have a noticeably shortened life expectancy. If operated in a continuous 122°F environment, the battery life could be shortened to less than one year, while at 75°F they would be expected to last three to five years. Battery charging above 104°F (40°C) also becomes a problem as the batteries should not be charged above this temperature. Some off-the-shelf UPS manufacturers offer wide temperature range battery options. The wide temperature range VRLA battery has been designed to operate over a -54° to +176°F (-65° to +80°C) range, but will still have a reduced life at temperature extremes. Charging is also not an issue at the elevated temperatures.

Operational Concerns

Proper qualification testing of any off-the-shelf UPS selected is imperative. Verifying the manufacturer's specifications is a good place to start, but must be performed in some areas with the worst-case scenario in mind. For instance, take the simple input voltage specification. It might be 120 Vac ±20% or 96 Vac to 144 Vac and one might assume that verifying operation between these voltages would suffice. The specification should not be taken by itself, but in the entire context of the other specifications that may be affected over the entire input voltage range. Beyond the battery mode testing, proper load testing of the UPS should be conducted. Proper load testing can be a real indicator of the quality and performance capabilities of a UPS. Load testing must also include overload testing to verify the proper protection capabilities have been incorporated and functional.

Overload testing also provides a good insight as to how the UPS handles differing overload conditions. For instance, a given UPS application may include powering a pump motor that has a very high inrush current demand. This demand may exceed the rating of a 3kVA UPS for a short period of time (less than 200 milliseconds). A 3kVA UPS from one manufacturer may have enough overload capacity to support the load without a problem. A UPS from another manufacturer may only sound an audible warning during the short overload period and recover. A UPS from a third manufacturer might sound a continuous alarm and turn off its output, requiring it to be totally shut down and restarted.

For load testing, both a linear and non-linear load with a 0.7pf should be used during the testing and the test results recorded with both loads. Much of the electronic equipment available today incorporates switch mode power supplies that typically have a non-linear input stage consisting of a rectifier and filter capacitors, giving the device an input power factor of about 0.7pf. These types of loads tend to gulp current toward the peaks of the sinewave. When several pieces of this type of equipment are connected to a UPS, the high non-linear current demand may cause problems for a poorly designed UPS.

DC Offset Measurement

Beyond the specifications, there are a couple of key parameters to look at. The first is the output DC offset. Is the zero crossing point of the output sinewave at zero volts or has it shifted at some DC level? DC offset is a very important consideration, especially if the UPS is to have a transformer connected to its output. DC offset should be measured with both no load and full load connected to the UPS output. A good UPS will have a DC offset of less than 50mv. DC offsets of more than a volt should be a matter of concern. Figure 3 shows a DC offset measurement circuit for an on-line UPS.

The second parameter to be verified is the input inrush current when the UPS is initially turned on. On-line UPS units typically have an input stage similar to the switching power supply previously discussed. When the UPS is initially turned on, large input filter capacitors charge, which causes an initial short duration current spike that can be quite high (over 75A) if not properly addressed in the UPS design. If a toridal input transformer is incorporated into the UPS design, the inrush current can be much higher. When installed in the field, this can result in nuisance circuit breaker tripping when the UPS is turned on. Figure 4 compares the waveforms of controlled inrush current versus an uncontrolled one.

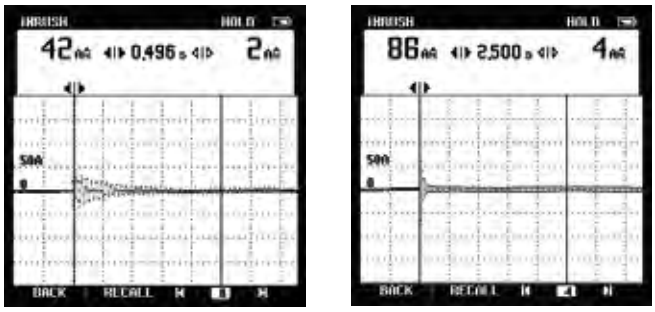

Figure 4

When the UPS is first turned on, large input filter capacitors charge, which causes an initial short duration current spike that can be quite high (over 75A) if not properly addressed in the UPS design. Compared here are the waveforms of a controlled (left) inrush current versus an uncontrolled one (right).

In conclusion, verifying the individual specifications without a clear understanding of how the specifications interrelate will not give a clear picture of the UPS unit's true overall performance, thermal margins, problems, reliability or suitability for a specific application. The evaluation criteria stated only covers some of the key areas of concern, but should give a clear indication if the off-the-shelf UPS is worthy of more investment of time and further qualification testing.

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Coming Next Month

COTS JOURNAL

- *Data Recording Architectures Revamp for Advanced Signal Processing.* Choosing a data recording solution for an advanced signal processing military system might seem a straightforward task. But in reality it ranks among the more critical and challenging decisions engineers have to make. Consider the multitude of components found in modern sensor systems and the differing characteristics of those components. Pairing sensor acquisition/analysis subsystems with recording and storage subsystems requires consideration of interconnect pre-processing and reliability issues. Articles in this section step readers through these issues and highlight the current crop of data recording systems.
- *MicroTCA and AMC in Military Systems.* MicroTCA is gaining interest as a compact, integrated solution, using the growing selection of AMC mezzanine cards essentially as slot cards. Articles in this section examine the latest trends along those lines, as well as an update on efforts to ruggedize MicroTCA.
- *The Ever Growing Systems Cooling Problem—A Technology Update.* There's just no avoiding the trend toward processors and other key components ramping up in wattage. And more power means more challenges dissipating heat. Exotic techniques such as spray-cooling and liquid-cooling are all on the table as possible ways to attack the cooling challenge. Articles in this section touch on all these present-day and future cooling solutions.
- *PXI,VXI and LXI Boards.* For complex, high-performance military systems, the PXI bus form factor, and its older cousin VXI, have become staples as instrumentation and test solutions. Now the LAN-based LXI form factor is the latest stepchild in this space to emerge on the scene. This Tech Focus section updates readers on the latest trends in these technologies along with a focused product album of representative boards in these architectures.

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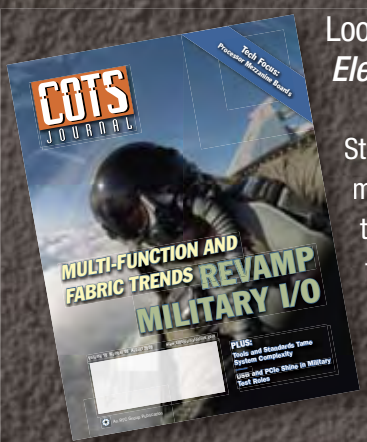

Look for a special section this October: ***Industry Analysts Plot Future of Electronics/Computers in Military.***

Strong evidence is mounting that the overall DoD budget will shrink in coming months and years. But even as the political landscape changes and forces within the government drive that budget down, the embedded computer component of the overall DoD budget is going to increase dramatically. Top Analysts from Frost & Sullivan, Venture Development, The Gartner Group and COTS Journal's own editorial staff will plot out the industry's future. Don't miss this unique reference resource.

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COTS JOURNAL

Editorial

Jeff Child, Editor-in-Chief

A Sea of Shipbuilding Troubles

There's an interesting tidbit I found one day in my family genealogy: During the American Revolutionary War, the Child family used to own and operate a shipbuilding company in Massachusetts. Included in that page of the genealogy was a bit about how apparently my shipbuilder ancestors had to burn all the boats in their yard in order to keep them out of the hands of the advancing British troops.

It would be nice if that shipbuilding legacy in my DNA gave me a leg up in understanding the complexities of today's super-advanced Navy shipbuilding programs like the DDG 1000 Zumwalt class destroyer. Unfortunately that's not the case. That said, I do my best to periodically get on the phone with those knowledgeable about the program and try to keep track of its development. Recent news about the DDG 1000 program is not good. Delays and budget overruns have plagued it. And it appears that, from what I hear, the problem at the heart of these woes is something I am VERY familiar with: software development that takes longer than expected and the consequent mismatch that creates within the system hardware development schedule. As someone who has covered embedded computing technology my whole career, that's a familiar tale to me.

The detail design and construction of DDG 1000 was preceded by a technology development phase—under the designation DD(X) that has been going on for several years and continues today. The Navy sees DDG 1000 as the technology driver for the fleet and a bridge to future ship capability, so what happens with DDG 1000 has a lot of impact. The Zumwalt class destroyers are designed to act as multimission surface combatant ships to provide advanced land attack capability to support forces ashore. The schedule calls for the Navy to take ownership of the first two Zumwalt-class destroyers—DDG 1000 and DDG 1001—in 2013 and 2014, respectively. The plan was for a total of seven to be built, but last month the Navy decided DDG-1000 Zumwalt class will be discontinued after the first two ships have been completed.

A number of vendors from the embedded industry are involved in the DDG 1000. For example, GE Fanuc Embedded Systems supplies SBCs and multifunction PMCs sporting three Gbit Ethernet ports to the program. The ship's network is called the Total Ship Computing Environment Infrastructure (TSCEI). The GE Fanuc boards will be used specifically in Raytheon's Distributed Adaptation Processor (DAP), which bridges the VME64x-based embedded computing systems used for vertical launch of missiles, gun systems, radar, sonar, decoys, and supplies power to the TSCEI.

Shipbuilding gets tricky when various components don't keep pace with the master construction schedule for a ship. The efficient way to do it is to build the ship in modules, maximizing the amount of construction, test and outfitting completed in shipyard shops and in the dry dock while at the same time minimizing work to be performed once the ship is in the water. If equipment is not ready in time for installation, the shipbuilder will have to work around the missing equipment. Once units are installed, access to internal ship compartments becomes more difficult.

Many of the most challenging phases of the DDG 1000 software development still lie ahead. Reportedly problems were encountered in testing the most recent software release, meaning more delays. Delays in software delivery would disrupt plans for activating the ship's critical systems as well as its combat systems, and delay delivery of the ship and its combat systems to the Navy.

A recent restructuring of the program opened up some time for producing, installing and testing key combat systems and the software that supports these systems—and in doing so called for doing more work later in construction and after ship delivery. Some key systems, including the dual-band radar, haven't been fully demonstrated as planned. Meanwhile, the integrated power system will be produced and installed before land-based testing is complete. All that increases the risk that problems discovered during testing will require expensive rework to incorporate fixes later on.

There's a lot to be learned from the DDG 1000 program's trouble. And the Navy, the Congress and the GAO are all looking at it under the microscope. In testimony before the House Subcommittee on Seapower and Expeditionary Forces, Committee on Armed Services, Paul L. Francis, Director of Acquisition and Sourcing Management for the DoD said, "… while managers may know what it takes to put an executable business case together, compromises in judgment have to be made to bring the business case in conformance with competing demands. For example, in a program like the DDG 1000 that undertook multiple technical leaps to meet challenging requirements, yet also had to deliver in time to match shipyard availability, pressures existed to make optimistic assumptions about the pace of technology maturity."

I've spoken before in this column about advanced military programs that seem, in my humble opinion, to jump too quickly into the engineering and manufacturing stage, without leaving ample room for technology discovery and maturity. And I'm getting the feeling it won't be the last time. ■

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